# A Guide to VFD Operation

- **1** Operating Principles
- 2 Construction
- **3 Drive Characteristics**
- 4 Timing Characteristics
- 5 Filament Power Supply
- 6 Filament Bias Voltage
- 7 Grid and Anode Power Supply
- 8 Precautions

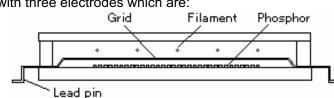


The contents of this document are subject to copyright and may not be amended or included in other documents or media without the express permission of Noritake Co., Limited, Japan. Revised 28th July 2001

# 1. VFD Operating Principles and Structure

The VFD is a kind of triode vacuum tube with three electrodes which are:

- Cathode Filament(s)
- Control Grids
- Illumination Anodes



The electrons emitted from the cathode filaments are controlled by the grids. When the grid is supplied with a positive voltage, it attracts the negative electrons, diffuses them and, due to their acceleration, many flow through the grid mesh towards the anode (opposite charges attract). However, when the grid is supplied with a negative voltage, it repels the negative electrons and prevents them from reaching the anode (similar charges repel).

The illuminating anodes are coated with phosphor which emits light when hit by the electrons. Each anode forms a segment or dot, which collectively form individual characters. When an anode is supplied with a positive voltage, it will attract the electrons which have been accelerated through the grid. The segment emits light when these electrons impact on the phosphor coating. Alternatively when anodes are supplied with a negative voltage, they will repel electrons from their phosphor coating and therefore remain un-illuminated.

By selecting combinations of illuminated segments, the desired digit or character can be formed.

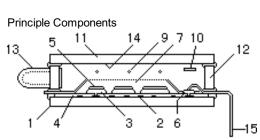


Fig.2 Frame and Hybrid Type



1.Glass Substrate (Anode Plate)10.Getter2.Conductive Layer11.Face Glass (Cover Glass3.Anode (Base)12.Spacer Glass4.Insulation Layer13.Evacuation Tube5.Phosphor (Display Pattern)14.NESA (or ITO) coating6.Conductive Paste15.Lead Pin7.Grid Mesh16.Mold Resin8.Conductive Frit Glass17.Solder9.Filament (cathode)18.Frit Glass				
3.Anode (Base)12.Spacer Glass4.Insulation Layer13.Evacuation Tube5.Phosphor (Display Pattern)14.NESA (or ITO) coating6.Conductive Paste15.Lead Pin7.Grid Mesh16.Mold Resin8.Conductive Frit Glass17.Solder	1.	Glass Substrate (Anode Plate)	10.	Getter
4.Insulation Layer13.Evacuation Tube5.Phosphor (Display Pattern)14.NESA (or ITO) coating6.Conductive Paste15.Lead Pin7.Grid Mesh16.Mold Resin8.Conductive Frit Glass17.Solder	2.	Conductive Layer	11.	Face Glass (Cover Glass)
5.Phosphor (Display Pattern)14.NESA (or ITO) coating6.Conductive Paste15.Lead Pin7.Grid Mesh16.Mold Resin8.Conductive Frit Glass17.Solder	3.	Anode (Base)	12.	Spacer Glass
6.Conductive Paste15.Lead Pin7.Grid Mesh16.Mold Resin8.Conductive Frit Glass17.Solder	4.	Insulation Layer	13.	Evacuation Tube
7. Grid Mesh 16. Mold Resin   8. Conductive Frit Glass 17. Solder	5.	Phosphor (Display Pattern)	14.	NESA (or ITO) coating
8. Conductive Frit Glass 17. Solder	6.	Conductive Paste	15.	Lead Pin
	7.	Grid Mesh	16.	Mold Resin
9. Filament (cathode) 18. Frit Glass	8.	Conductive Frit Glass	17.	Solder
	9.	Filament (cathode)	18.	Frit Glass

# 2. VFD Construction

Noritake Itron VFDs have several methods of construction. The basic model is that of the frame type construction. The other variants are specific to the product type and are described in more detail in the relevant application notes associated with CIG (Chip in Glass Driver), Active Matrix and Rib Grid VFDs.

The Grid Rim, Filament Support and Lead Pins are provided on a single metal frame. The ends of the Grid Rim are extended to the outside of the envelope, and are formed as lead pins for the Grids. The Anode leads are extended into the envelope to connect with the pads which are placed on the glass substrate. Both ends of the filament are welded to the Filament Support and Anchor with the appropriate tension.

The Frame is assembled with the Face Glass and Glass Substrate (Anode Plate). The Lead Pins are tinned and formed into a suitable shape for PC Board assembly. FRAME-Types require press formed metal dies for construction. They offer good production yield and high reliability against various environmental conditions.

A hybrid of this construction mounts the grids directly on the glass substrate which allows complex grid patterns.

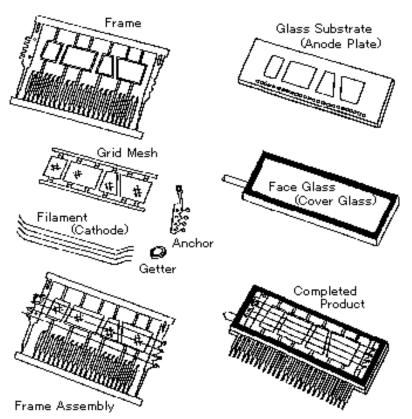


Fig. 3 Frame Type Construction

# 3. VFD Drive Characteristics

### 3.1 VFD Driving Modes

Two drive modes are possible with VFD which are referred to as static and multiplexing. The mode is dependent upon the pin-out of the anode segments and grids of the specific VFD.

### 3.1.1 Static Drive

In a static display, each anode segment is individually connected to a lead pin and a single grid covers all the display pattern in the VFD. This has the advantage in that it only requires 10 to 15 volts DC to illuminate the display and, in some cases, illumination is possible using standard 12 volts C-MOS logic. The major disadvantage with static mode is the need for more lead pins and IC drivers as the number of anode segments increases. Fig.4 and 5 show the basic construction and drive circuit.

# 3.1.2 Multiplex Drive (Dynamic Drive)

To minimize the number of pin connections and driver chips, the majority of VFD's use the multiplexing drive method. As shown in Fig.6, corresponding anode segments are connected in common under each separate grid, with each in turn being connected to a data line. Each character has its own separate grid which not only diffuses the electrons from the filaments, but also controls the selection of the character position in a "time share" multiplexing cycle. The duty cycle 'on time' of each character will determine the appropriate operating voltage required to provide sufficient luminance. Fig.7 shows the basic driving circuit.

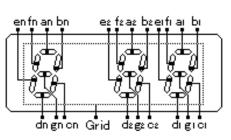


Fig.4 Static Drive VFD

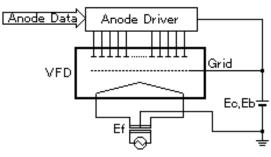


Fig.5 Driving Circuit of Static Drive VFD

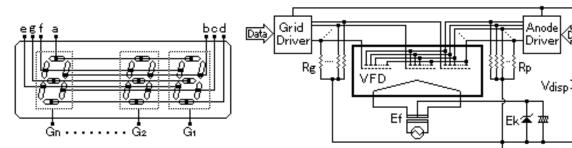


Fig.6 Multiplex Drive VFD

Fig.7 Driving Circuit of Multiplex Drive VFD

The timing T1 in Fig.8 shows that when Grid 1 (G1) is ON and data lines Pb and Pc are ON under Grid 1, with all the other grids OFF, the numeric character '1' will be displayed. After the time period T1, Grid 1 is turned OFF and the voltages on the anode data lines are reconfigured to suit the requirements of Grid 2. Grid 2 is then turned ON. In the example, this will be the numeric character '2'. The scanning of Grid 1 to Grid n should be repeated at more than 100 times per second so that persistence of vision in the human eyes gives a stationary, solid display without any flicker. The number of grids and anodes is optimized to reduce the number of lead pins to a minimum. Other factors may be important so the multiplexing drive can be a duplex drive, where the display is separated under two grids, taking advantage of requiring fewer drive chips than static mode and a lower drive voltage than that required by an ordinary multiplexing mode.

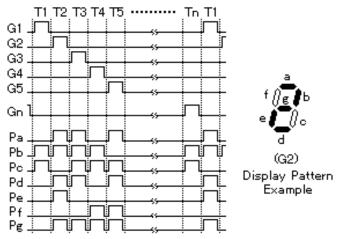


Fig.8 Example Timing Chart of Multiplex Drive VFD

### 4.1 Grid Scanning Frequency (Refresh Frequency)

When multiplexing, the selection of a slow grid scanning frequency may cause a flickering effect, which is a result of the optical beat generated by the on and off luminescent cycle and the image retention of the human eyes. As the anode and grid current is varied by the filament voltage level, you may observe flickering when the beat frequency between the AC filament (or pulse) and the grid scanning is 40Hz or less. Therefore we would suggest combinations as per Table 1.

Alternatively, high frequency scanning may cause problems because of insufficient pulse width for luminance against blanking time. If flickering is caused by this, avoid a scanning frequency between 250Hz and 500Hz.

### 4.2 Inter-Digit Blanking

Another potential hazard in multiplexing is ghosting. This phenomena is caused by decaying grid signal pulses which are caused by stray capacitance between VFD electrodes and display drivers. If the grid timing overlaps the following grid and anode signal pulses, as shown in Fig.9(a), ghost illumination appears at un-addressed anode segments.

To overcome this problem, an inter-digit blanking time should be added between grid pulse timings as shown in Fig.9(b). Generally the inter-digit blanking time should be approximately 10 to 50usec, but this can vary depending on the delay time. Delay time occurs when high value pull down resistor type drivers are used or when the drive circuit is situated away from the VFD. We recommend that an appropriate inter-digit blanking time is utilized on the grid signal only, rather than on both grid and anode signals.

Table 1 Grid Scanning Frequency

Filament Frequency	Grid Scanning Frequency
50Hz	90Hz or above
60Hz	100Hz or above
Frequency above 10kHz	60Hz or above

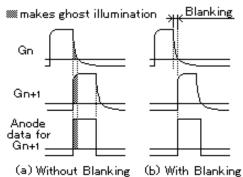


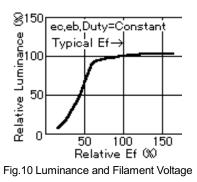
Fig.9 Inter-Digit Blanking

# 5. Filament Power Supply

#### 5.1 Filament Voltage

Luminance varies with the filament voltage (Ef) as shown in Fig.10. Since the lifetime of a VFD is dictated by the extent of evaporation of oxide materials coated onto the tungsten filament wires, it is critical that the filament voltage is supplied within the specified ratings.

Current drain from the anodes and grids to the filaments can cause ghost illumination so a bias voltage is applied to the filaments to raise them above ground. This is described later.



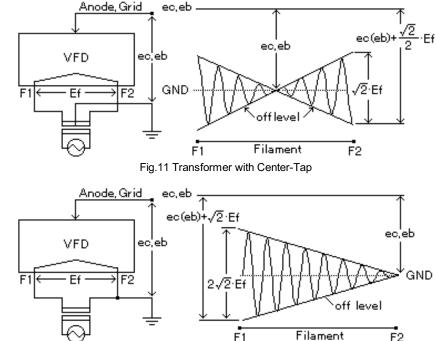


Fig.12 Transformer without Center-Tap

### 5.2 AC Filament Drive (50 or 60Hz)

Generally, the transformer is the most popular device utilized to supply the filament voltage (Ef) with a 60(or 50)Hz sine wave which also has a center-tap for cathode bias as shown in Fig.11. The center - tap technique is used to prevent luminance slant i.e. difference in brightness from one side of the display to the other.

Using a transformer without this center-tap can not only cause luminance slant but also ghost illumination due to exceeding the amplitude of the filament voltage in excess of the specified cut-off bias voltage rating.

# 5.3 Pulse Filament Drive (High Frequency RMS)

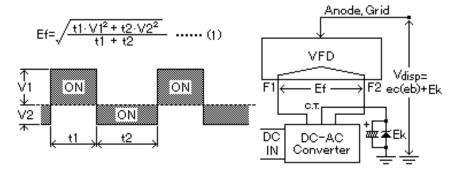
In the case of a DC or battery power supply, a pulse wave form for the filaments can be generated from a DC to AC converter. The concept of pulse voltage supply to the filament is the same as AC filament drive. In either case Noritake still recommends the DC to AC converter with a center-tap as shown in Fig.13. Please note that the pulse voltage should be calculated as an RMS (root mean square) value from the wave form as shown in formula (1).

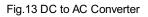
However, a 1/2 duty factor should be set, and the peak to peak pulse wave form should be 1.5 times or less than the RMS value. A frequency range of 10kHz to 200kHz is recommended.

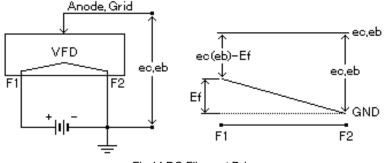
# 5.4 DC Filament Drive

If a DC filament drive is adopted, a potential difference between the anode and grid voltage will be apparent as a luminance slant across the display as shown in Fig.14. This shows brighter luminance at one side of the display due to the DC voltage drop. In order to avoid this problem, special measures are applied during display construction and the polarity (+,-) of the filament or grid terminal is specified. However, this is only possible for relatively short length VFD's.

**Note:** Please consult Noritake in advance before designing DC or DC pulse filament drive circuits.



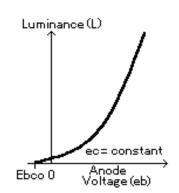






# 6.1 Cut-Off Characteristics (Grid/Anode Cut-off Voltages)

Luminance (L) varies with the anode voltage (eb) as shown in Fig.15 when the grid voltage (ec) is a constant. Luminance also varies with the grid voltage as shown in Fig.16 when the anode voltage is a constant. To completely turn off the luminescence at the un-addressed display segments, a negative voltage shall be applied to the un-addressed anodes and grids with respect to the filament. These negative voltages are called anode cut-off voltage (Ebco) and grid cut-off voltage (Ecco) respectively. The cut-off voltage-varies depending on each type of display due to various differences in filament voltage and wave form. Please note that the cut-off voltage quoted in each particular specification is based upon the AC voltage being supplied via a transformer complete with center-tap.





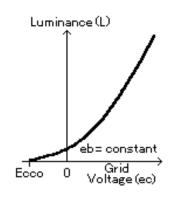


Fig.16 Grid Voltage and Luminance

# 6.2 Filament Bias Voltages (Ek)

The filament bias voltage (Ek) is a voltage applied to the filament center-tap in order to cut off background illumination when the anodes and grids are not addressed. The 'off' anode and grid voltages remain negative with respect to the filament. The total supply voltage Vdisp is ec(eb) + Ek. (In the case of CIG displays, the Ek is included in VDD2.)

In typical driving circuits, a zener diode supplies the Ek as shown in Fig.17. The cathode bias (Ek) for filament center-tap is higher than that specified for the grid cut-off voltage (Ecco). Usually, the Ek is set at the same value as MIN voltage of Ecco shown in the specification or a slightly large value when utilizing a filament center tap (F.C.T.). If a center-tap is not available, a virtual center-tap with resistors is one acceptable alternative.

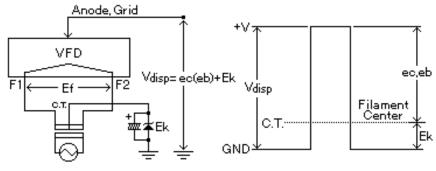


Fig.17 Cathode Bias

# 7. Anode and Grid Power Supply

### 7.1 Circuits

As shown in Fig.17, the power supply voltage for anode and grid should be Vdisp = ebc+ Ek (Volts) which is the sum of grid/anode voltages (ebc=ec=eb) and cathode bias voltage (Ek). This output voltage must be stabilized otherwise its ripple may coincide with the grid scanning frequency and may cause flickering of the display.

### 7.2 Relationship between voltage and brightness

A peculiarity of VFD is that both grid and anode are active when high. If there are any limitations with the power supply and/or driving software, the supply voltage or duty factor may not be available to meet the specified value (typical ratings). In this case, you may re-calculate the ratings using the following formula.

L = K \* ebc^2.5 \* Du ...... (2)

K: constant of each display ebc: anode and grid voltage (ec=eb) Du: Duty factor

For example, when the duty factor is beneath the specified rating, a specified brightness rating can be achieved by modifying  $ebc^{2.5*}Du$ . If Du(TYP) and ebc(TYP) are as specified, and Du(x) and ebc(x) are modified values than the related expression is as follows:

 $L = K * ebc(TYP)^{2.5} * Du(TYP) ..... (3)$ 

 $L = K * ebc(x)^{2.5} * Du(x) \dots (4)$ 

 $ebc(TYP)^{2.5} / ebc(x)^{2.5} = Du(x) / Du(TYP) \dots (5)$ 

### **IMPORTANT!**

ebc(x) and Du(x) can be calculated as above, however, ebc(x) must be within the maximum ratings stated in each particular specification.

### 7.3 Brightness Control (Dimming)

High brightness is the main characteristic of VFD. However, in certain applications, it may be desirable to offer dimming capabilities for operation in dark environments. In such a case, the brightness level can be controlled by reducing the duty factor as shown in Fig.18. The brightness level can be adjusted in proportion to the luminous 'on' time to 'off' time. However brightness dimming by reduction of filament voltage or anode/grid voltage is not recommended because this may cause uneven illumination.

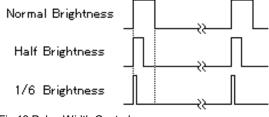


Fig.18 Pulse Width Control

# 8. Precautions

The data for electrical characteristics, reliability and lifetime expectancy has been based on typical driving conditions. When designing circuitry, apply the typical rate of driving voltage or, if the voltages fluctuate, the minimum and the maximum values of the driving voltage should be set within specified ratings. Exceeding any of the maximum ratings may cause damage to the display, or driving below minimum ratings may cause insufficient brightness. Displays used under anything other than specified conditions will be defined as out of warranty.