DECOUPLING IN HIGH-SPEED ENVIRONMENTS

INTRODUCTION

The purpose of this application note is to make recommendations regarding decoupling in a high speed environment.

Why decoupling ?

Faster edges, wider busses, more sensitive devices, and higher clock rates all demand careful decoupling of the power supply. High-speed switching environments generate noise on power lines or planes due to the charging and discharging of internal and external of an integrated circuit. The instantaneous current generated with the rising and falling edges of the output causes the power supply to ring. This behavior can violate the Vcc recommended operating conditions or generate false signals. A simple solution, a bypass capacitor, must be utilized to prevent such a problem.

Definitions

Decoupling:

The art and practice of breaking coupling between portions of systems and circuits to ensure proper operation.

Bypassing:

The practice of adding a low-impedance path to shunt transient energy to ground at the source. Required for proper decoupling.

A bypass capacitor stores an electrical charge that is released to the power line whenever a transient voltage spike occurs. It provides a low-impedance supply, thereby minimizing the noise generated by the switching outputs of the device.

BYPASSING CONSIDERATION

A system that does not utilize bypassing techniques can be affected by severe power disturbances and cause circuit failures. Several factors need to be considered when selecting local bypass capacitors. These factors include selecting the proper capacitor value, dielectric material, geometry and location of the capacitor in relation to the device.

Real Bypass Capacitor

Bypass capacitors are riddled with imperfections, capacitor performance varies widely.

Every capacitor includes a parasitic series inductance, called the lead inductance, package inductance, or mounting inductance. Its impedance goes up at very high frequencies.The best way to get very low inductance is to parallel several small capacitors all around the entire board.

Three factors will dominate the impedance between power and ground:

- At low frequencies, the inductance of power distribution wiring dominates.
- At middle frequencies, the impedance of a board-level bypass capacitor dominates.
- At high frequencies, the impedance of a distributed capacitor array dominates.

Surface-Mounted Capacitor

Surface-mounted capacitors solder directly to a circuit board with no intervening leads, therefore decreasing lead inductance significantly.

Surface-mounted package sizes have names associated with their length and width. The Equivalent Series Resistance (ESR) of a surface-mounted capacitor may not be lower, but the lead inductance drops to the range of 1 nH. Very small packages such as the 0805 have even less series inductance.

All capacitors also includes a parasitic series resistance, called the Equivalent Series Resistance (ESR). It acts like the lead inductance to defeat the effectiveness of a capacitor. ESR is a real-valued impedance and is not a strong function of frequency. It acts like an ordinary resistor in series with the capacitor. ESR value appears on a capacitor manufacturer's data sheet and varies widely.

Bypass capacitors are also temperature-sensitive. The dielectric properties can change significantly with temperature, leading to wide swings in capacitance. See the "Capacitor Dielectric" section in this document.

Bypass capacitors can blow up or short out if exposed to too high of a voltage. See the "Voltage Ratings and Lifetime" section in this document.

Capacitor Type

In a high-speed environment the lead inductance of a bypass capacitor is critical. High-speed switching of a device's outputs generates high frequency noise on the power lines or planes. These harmonics (>100MHz) cause the capacitor to act as an open circuit. Therefore, bypassing the power planes from the device's internal noise requires very small inductance capacitors. Multilayer ceramic capacitors offer negligible internal inductance.

Capacitor Placement

To provide the lower-impedance path for the transient current to be grounded, a bypass capacitor should be placed as close as possible to the power pin of the device and on the same side of the PCB as the Integrated Circuits (ICs).

This will reduce the resulting inductance, and will allow the capacitor to operate more efficiently and avoid noise on the power planes.

Output Load Effect

Capacitive loads, added with high-speed edge signals, result in bigger transient current and possible power oscillation.

When driving large capacitive loads, more charge must be supplied to the output load, resulting in slower edges. However, if the bypass capacitor is not capable of providing the needed charge, power planes start to ring and eventually to oscillate, causing different power references across the board. These oscillations can be up to 2 to 3V peak to peak amplitude, and can be reduced, limiting output load capacitance.

Capacitor Size

When choosing appropriate bypass capacitors, the most important parameter is the capability to supply instantaneous current when needed.

1. Calculate using the following equation:

   $$C = \frac{I \times N \times dt}{dV}$$

   I is the amount of current needed to switch one output from low to high, *N* is the number of outputs switching, *dt* is the time required for the capacitor to charge the line, and *dV* is the drop in Vcc that can be tolerated.

2. When maximum pulse slew rate is provided by the capacitor manufacturer, you can calculate the maximum current allowed.

   For example, a 100 nF capacitor rated at 50V/µs can supply 5 Amps (I = C dv/ dt).

Capacitor Dielectric

Bypass capacitors can be classified by their dielectric material. All dielectric materials have a high dielectric constant, in the order of 1,000-10,000 or more. Unfortunately, the materials with the highest dielectric constants also have the worst temperature coefficients.

Given a particular dielectric material, the volume of a capacitor is roughly proportional to its capacitance and to its maximum voltage rating.

Aluminum Electrolytic Dielectric

Aluminum electrolytic dielectric capacitors are the capacitors used most often for board-level bypass.

ESR is extremely sensitive to temperature, aluminum electrolytics do not work well in cold applications.

Z5U Dielectric

Monolithic ceramic capacitors are constructed from layers of metal sandwiched between ceramic insulating layers. The Z5U dielectric material has a higher constant than X7R but worse temperature and aging properties.

X7R Dielectric

X7R is another dielectric material used to construct monolithic capacitors. The X7R dielectric material has a lower constant than Z5U but better temperature and aging properties.

Voltage Ratings and Lifetime

Failure in capacitors is a statistical phenomenon and is accelerated at high voltages. When a manufacturer quotes a working voltage rating, it doesn't mean the capacitor will never fail if operated at that voltage. It only means it tends not to fail very often if operated at that voltage or below.

When operated below their maximum working voltage, capacitors show markedly longer useful service lives. A 50% voltage derating may significantly improve a capacitor's expected lifetime.

DECOUPLING-CAPACITOR CALCULATIONS

To determine the value of the decoupling capacitor, you must estimate the instantaneous current required when all the outputs of an IC switch from LOW to HIGH, assuming a reasonable droop of the voltage on the capacitor. The charge stored on the local decoupling capacitor is:

$$Q = CV$$

Differentiating yields:

$$i(t) = \frac{dQ}{dt} = C\frac{dV}{dt} \qquad \textit{Equation 1}$$

The characteristic impedence of a typical transmission line is 50Ω. Lines with a heavy capacitive load have lower characteristic impedances.

Assume that the device is a 512K x 8 Fast SRAM, such as the White Microelectronics WS512K8-XXX. The outputs reach:

$$V_{CC} - V_t = 5V - 1V = 4V$$

V_t is the voltage threshold of CMOS technology devices

Each output requires 4V/50Ω = 80mA. Because the SRAM has eight outputs, it requires a total of 640mA during the rise times of the outputs.

Solving *Equation 1* for C yields:

$$C = \frac{I \times dt}{dV} \qquad \textit{Equation 2}$$

The last step is to assume a reasonable, tolerable droop in the capacitor voltage. Assume dV = 100mV. Additionally, the signal rise and fall times are 2ns. Substituting these values in *Equation 2* yields:

$$C = \frac{640 \times 10^{-3} \times 2 \times 10^{-9}}{100 \times 10^{-3}}$$

$$= 12.8 \times 10^{-9}$$

$$= 0.0128\mu F$$

It is standard practice to use 0.01 to 0.1-μF decoupling capacitors. A 0.1-μF capacitor can supply 5A under the conditions assumed in the preceding calculations.

HIGH-SPEED MEMORY DESIGN RECOMMENDATION

In high-speed memory design such as SRAM and Synchronous SRAM, power supply decoupling is an important factor in system reliability. When considering a high-speed design decoupling, keep in mind the following recommendations:

The inductance of a bypass capacitor is a determining factor which must be based on series inductance values.

Distribute bypass elements throughout the PCB, yet concentrate these elements close to the devices demanding large current transient.

- Planes should be used to distribute power and ground, but still require placement of capacitors close to the ICs power pins.
- Traces from the capacitors should go directly to the power and ground planes with leads as short as possible.
- A continuous ground plane with no avoidance areas is always required.
- Design the power and ground layers first.
- For mechanical reasons, lean toward using a symmetric arrangement of ground and power planes in your layer stack.
- Ground pins must be evenly distributed across all connector pin fields to prevent local ground upset due to transient currents. The number of connector ground pins in a connector is as follows:

  A minimum of one ground pin per inch of connector length or one per eight output signal lines.

Use the impedance method presented in this document, to determine the total inductance your design can tolerate, and carefully select low impedance capacitors.

SUMMARY

Bypass capacitors play an essential role in providing a reliable system. Absence of bypass capacitors can generate false signals and create major problems across an entire board.

Choosing a capacitor with negligible lead inductance can avoid unpredictable behavior at high frequencies. Locating capacitors close to the Vcc pins of devices will avoid further complications and eliminate ringing. It is always important to minimize the loop between Vcc pins, ground, and bypass capacitors. Finally, choosing the capacitor size, by using the mentioned method in this document, is a good approach.

Power supply oscillations can be controlled, limiting output load capacitance and choosing appropriate bypass capacitor value and placement.

References

1. Howard Johnson and Martin Graham, "High-Speed Digital Design: A Handbook of Black Magic" Englewood Cliffs.
2. Texas Instruments, "The Bypass Capacitor in High-Speed Environments"