

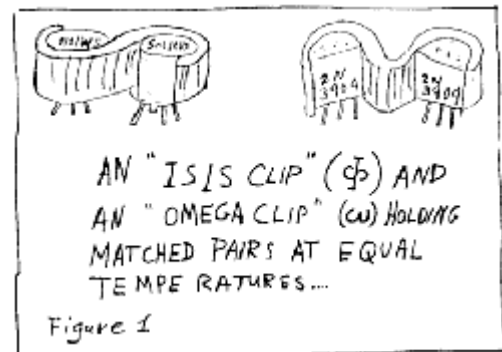


## The Best of Bob Pease

### What's All This Common-Centroid Stuff, Anyhow?

ONCE upon a time, we designers of op amps used to locate as many of the critical transistors as we could along the axis of symmetry. We put the input transistors right along the Center Line (CL) of the chip, or on a pc board along the CL of the board. We tried to put the output transistors on the CL, too, down at the far end of the layout. We realized that any heating from the output stage could cause significant, serious input errors. For my discrete layouts, I designed "ISIS Clips" and "Omega Clips" to keep the input transistors at the same temperature (*Fig. 1*).

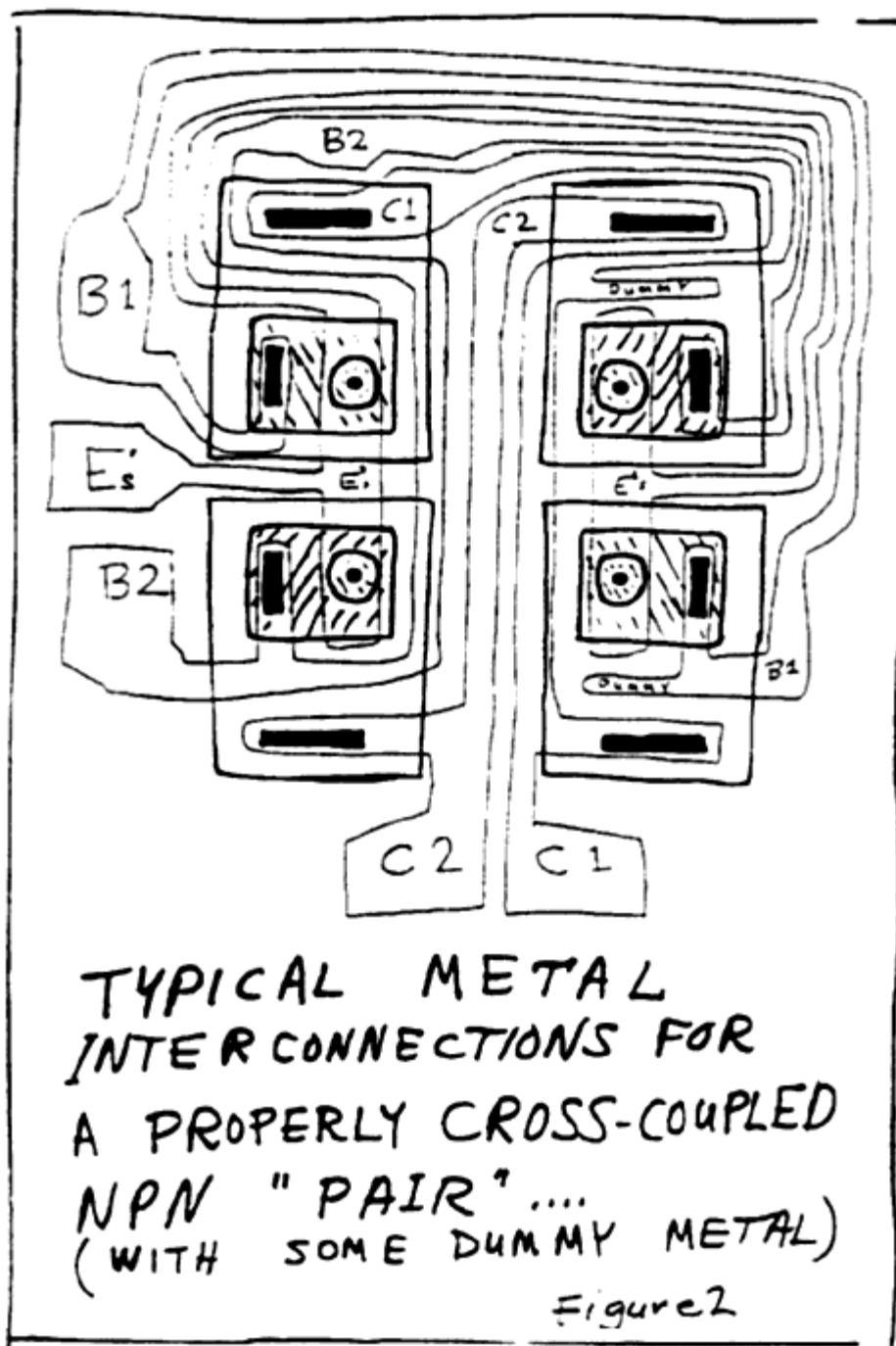
ISIS, the old Egyptian Goddess, was George Philbrick's inspiration. The K7-A6R array of op amps was called the "ISIS" computer. The symbol S with an I across it was a neat symbol for ISIS. Look at it again, and it's the PHI that's the symbol for PHILbrick. And if you are a fan of Positive Feedback, George Philbrick used to say that ISIS was her own mother. So I designed some little clips made of soft aluminum, with green paint for insulation all over them, in the shape of S -- an ISIS clip. This clip has rotational symmetry.



Conversely, an "Omega Clip" has mirror symmetry, like the Greek letter for omega (see Figure 1). We made these of the same soft aluminum, and the same green paint. Walter Kern made them up.

When monolithic op amps came along, there were some influences to "keep it simple, stupid". I designed a T52AH -- also labelled as Amelco's 809BE -- with just 10 transistors, which worked pretty well. But op amps with 20 or 30 transistors soon had just as good a yield. And they offered more features. So, we kept learning how to add more transistors for better performance.

But when the Fairchild  $\mu$ A725 came along, we designers were really puzzled. Why would anybody use FOUR input transistors? What the heck was George Erdi smoking? If you set up a diff amp with two transistors in parallel at the plus input and two transistors paralleled on the minus input, why would that give an advantage? But the specs showed real superiority -- low offset voltages, good bias currents, and low offset current. Hey, this was about 1971. Not many engineers were climbing inside their suppliers' ICs and studying the layouts. If you didn't, though, you could be stuck with a lousy layout. I know.



The basic feature of the  $\mu A725$  was the common-centroid layout of the input transistor "pair" (Fig. 2).

If you took those four input transistors and laid them out in an X pattern, it would be denoted by:

AB  
BA

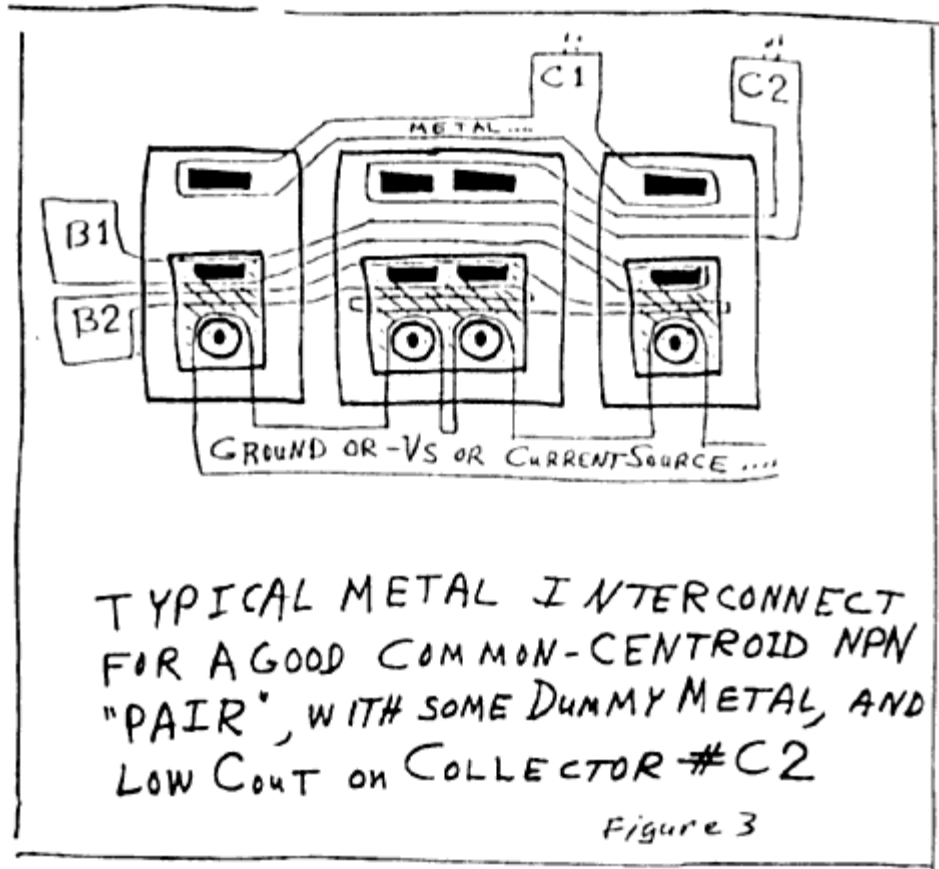
Connecting them properly in parallel, you can get the linear gradients of  $V_{os}$ , to cancel. And the gradients in beta to cancel. Gradients caused by heating from the output stage -- and even from

other asymmetrical sources of heat -- tend to cancel. Any linear gradients caused by imperfect die attach tend to cancel. (Nonlinear gradients do NOT get cancelled, of course, but these are usually small.) And these cancellations all happen thanks to a common-centroid layout, which is just another way to say that the "Center of Gravity" (CG) of one input "transistor" is at the same place as the CG of the other transistor. (I bet you can figure out that any geometry that is connected to metal labelled "B1" is a base -- if something is connected to "C2," that must be a collector ... )

There are many kinds of common-centroid layout, in addition to cross-coupling. You could lay out a "pair" of npns as ABBA. The "B" transistors in the middle not only reject gradients, but they can have smaller output capacitance, since they only need one tub. And in some cases, this long, skinny circuit (*Fig. 3*) may fit in your layout better than:

AB  
BA

In this example, the transistors are still connected as an ordinary differential pair. But if you connect the transistors to act as a current reflector by shorting C1, B1, and B2 together, and merging that metal, the interconnections become very simple.



Recently, I saw a technical article by some engineers<sup>1</sup>, claiming that they had a computer program that automatically provided good interdigitated and cross-coupled common-centroid layouts. "ALAS!" was what they called the program. I looked at their results. All I could say was, "Alas!!" The authors appeared to think that a layout of ABAB or AABBAABB or ABABABAB or even:

ABAB  
BABA  
ABAB

makes a "common centroid". When I apprised them of their error, they tried to argue that the magazine's computers had misrepresented their results. Uh-uh. They did not understand that *their* computers were clueless. Not only was it a bad program that generated poor layouts, but they did not even recognize that it was a bad layout. And, heck, you don't need a fancy computer to set up pairs or groups of transistors with common centroids. I do it all the time with groups of resistors, using just pencil and paper -- and lots of symmetry.

The Editor at the *Journal of Solid State Circuits* was a good sport, and gave me space for my

criticism of that paper<sup>2</sup>; and the authors' efforts to rebut my criticism<sup>3</sup>.

Often, there are significant matching errors when using transistors, or resistors, or capacitors, if common-centroid layout isn't used. There are always more-or-less linear gradients across a die. Bipolar transistors have gradients of  $V_{be}$  and  $\beta$ . If there's any temperature gradient caused by output device dissipation, that's going to hurt the  $V_{be}$  matching by  $2\text{mV}/^\circ\text{C}$ , if the input transistors aren't at identical temperatures. MOSFETs are afflicted by gradients in etching, in  $V_t$ , and in oxide thickness. Adjacent resistors can have poor matching due to gradients in etching and in sheet  $\rho$ . If you want your capacitor sets to match well, you must beware of gradients in etching and oxide thickness. Die stresses cause shifts that relate to linear gradients. Proper understanding of cross-coupling or other forms of "common-centroid" layout can be very valuable to help reject linear gradients across your die. An improper understanding of "common-centroid" layout can be amusing -- or pathetic. If you insist on cross-coupling components that are *not* critical, you can waste lots of die space.

Back in 1972, on Jim Pastoriza's AD550 Quad Current Switch, I observed some of the limitations of laying out a DAC's transistors all in a linear row. When some bits were switched ON or OFF, there were significant thermal tails. Linear mismatches also occurred, due to linear gradients in  $V_{be}$  and  $\beta$ .

I made my own layout for a monolithic Quad Current switch, with good common-centroid layout. It had 8,4,2, and 1 emitters -- and 2 emitters for the reference. What was the Patent number? 3,995,304? You can tell that it's an old number -- the patent has expired already. The emitters were laid out with the Most Significant Bit (MSB) emitters being A, the LSB as D, and the reference as R:

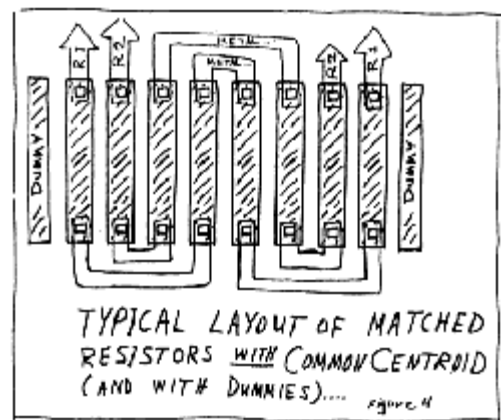
AAAA  
BBCR  
  D  
RCBB  
AAAA

I was able to convince myself that the  $V_{be}$  matching of this kind of layout was adequate for at least an 8-bit DAC -- without any emitter resistors. It may be as good as 10 bits, if I did some trimming. And much better, if emitter resistors were used. Heck, the first DAC I ever built was 15 bits *plus sign*.

If you use resistors, you should be aware that resistors made in a batch process tend to have linear gradients. So if you have four resistors in a row, and you want a good ratio, such as 1:1 (or 4:1), choose the two resistors in the MIDDLE. Put them in series, and take the resistors on the ends, and put them in series (or in parallel) and the ratio will tend to be more accurate. The tempco will be, too. This tends to hold true for thick-film, thin-film, or monolithic resistors. If you have eight resistors, the matching can get even better (Fig. 4).

Back in '86, Dennis Monticelli asked me which layout I would recommend for the input of his LMC660 op amp:

ABAB      ABBA  
BABA vs. BAAB  
ABAB      BAAB  
BABA      ABBA



Where's the advantage?

I told him they were both good, but I sort of liked the first option. The offset of this op amp set new standards for accuracy of MOSFET inputs. Never a dull moment!!!!

All for now. / [Comments invited!](#) (rap@webteam.nsc.com)  
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References:

1. Bruce, J.D., *IEEE Journal of Solid State Circuits*, Feb. 1996, p.271-274.
2. Pease, R.A., *IEEE Journal of Solid State Circuits*, Sept. 1996, p.1364.
3. Bruce, J.D., *IEEE Journal of Solid State Circuits*, Sept. 1996, p.1364.

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RAP's 1997 Comments:

I got a nice note from Dave Fullagar, the guy who invented the  $\mu$ A741. He said that the  $\mu$ A725 was the first amplifier to use the cross-coupled inputs, so I changed the text to agree with his facts.

(In the original version I said it was a  $\mu$ A714, but that came later.)

-- rap

