Qualcomm SBI Interface

Serial Bus Operation

The MSMxxxx device's SBI Master controller drives the SBI Slave units of the IFR,RFR,RFT and PMxxxx modem devices. The falling edge of SBST indicates the beginning of a serial data transfer. SBST goes high at the end of a completed data transfer. A data transfer operation is terminated at any time by forcing SBST to a high state. Serial data on the SBDT line is latched on the falling edge of the SBCK signal. SBDT changes state only when SBCK is low. All three lines of the SBI must be high for at least one clock period in order to initiate a new data transfer. Data on the SBDT line is always sent MSB first, LSB last. During the ninth clock cycle, the data line is released by the driver and is pulled high by an external 8 kΩ pull-up resistor.

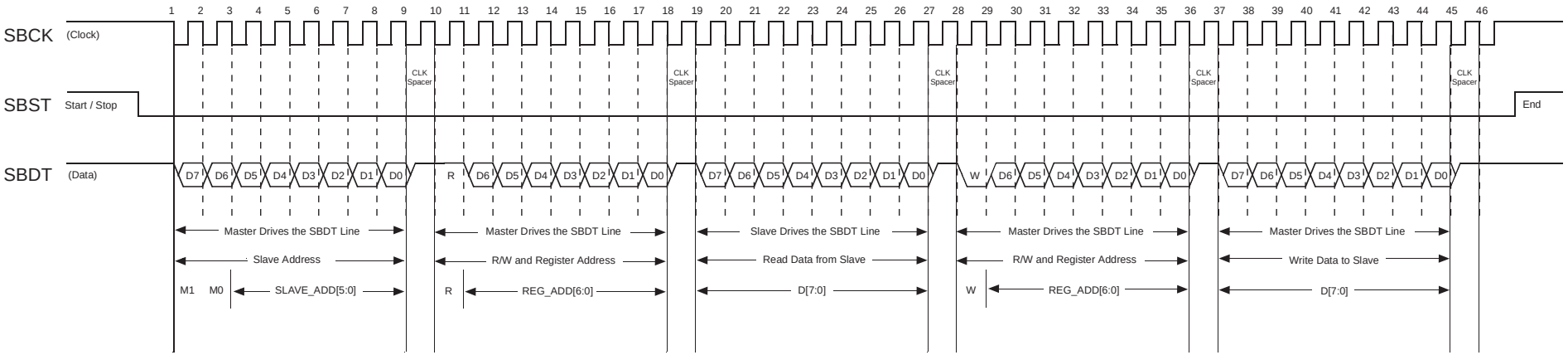
Slave Address Format

The first 9 bits sent on the serial bus after SBST goes low address the slave device. The first two bits of the SLAVE_ADD byte (SLAVE_ADD[7:6]) indicate the transfer mode. The next six bits (SLAVE_ADD[5:0]) are the unique address device being addressed, which is ignored by all other devices on the SBI. The ninth bit (REG_ADD[7]) configures the transfer as either read or write.

Fast Transfer Mode (SLAVE_ADD[7:6] = 01) is intended for data transfer to and from slave devices tied to the SBI. Data can be both read and written in the same transaction. The Fast Transfer Mode message format is shown in Figure 2.

The MSB of REG_ADD, (REG_ADD[7]) is used to set up the slave for reading or writing. When this bit is set (1), the SBI is reading from the slave device. When this bit is clear (0), the SBI is writing to the slave device. During a data transfer when the SBI changes from writing to reading, the SBDT line is released and the addressed slave device takes control of the SBDT line for the next eight SBCK cycles. Throughout the bidirectional data transfer, the MSMxxxx device's Master SBI Controller retains control of the SBCK line and keeps SBST low.

The seven LSBs of REG_ADD (REG_ADD[6:0]) can address up to 128 registers in a slave device. Afterwards, 8 bits of data (Data[7:0], Figure 2) are sent by either the Slave or Master depending on the state of the R/W bit, REG_ADD[7]. At this point either an additional REG_ADD[7:0] byte can be sent, or the transaction terminated with SBST going high. Address location 0x01 contains the Slave device identification number. Figure 1 illustrates the data transfer process.



I3Q Protocol:

1. Transactions are initiated by pulling SBST low.
2. Transactions are terminated/completed by taking SBST high.
3. All changes in the state of SBDT occur while SBCK is low.
4. First bit of data is latched on the second falling edge after SBST has gone low.
5. Data transmissions are always MSB first to LSB last.
6. The first 8 bits on the data bus address a slave.
7. Data may be both read and written within the same transaction.
8. There is an additional spacer clock cycle allocated for every byte transmitted.
9. During the clock spacer time, no master or slave drives the SBDT bus.

Figure 1: SBI Serial Data Transfer

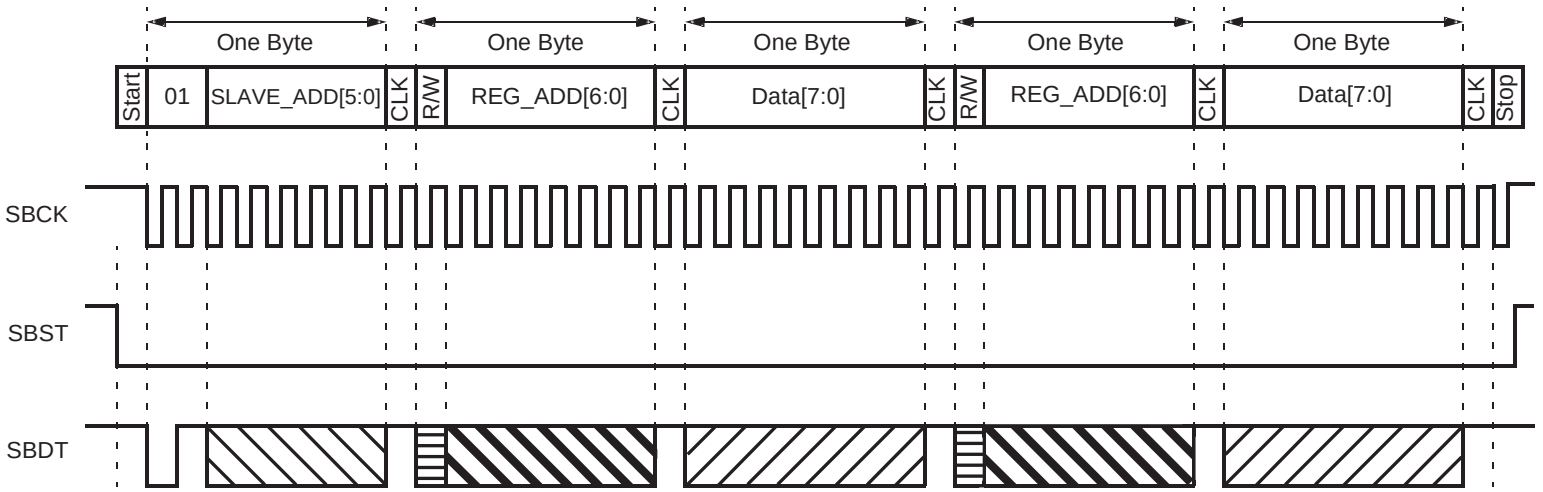


Figure 2: Fast Transfer Mode Message Format

SBI Bus Timing

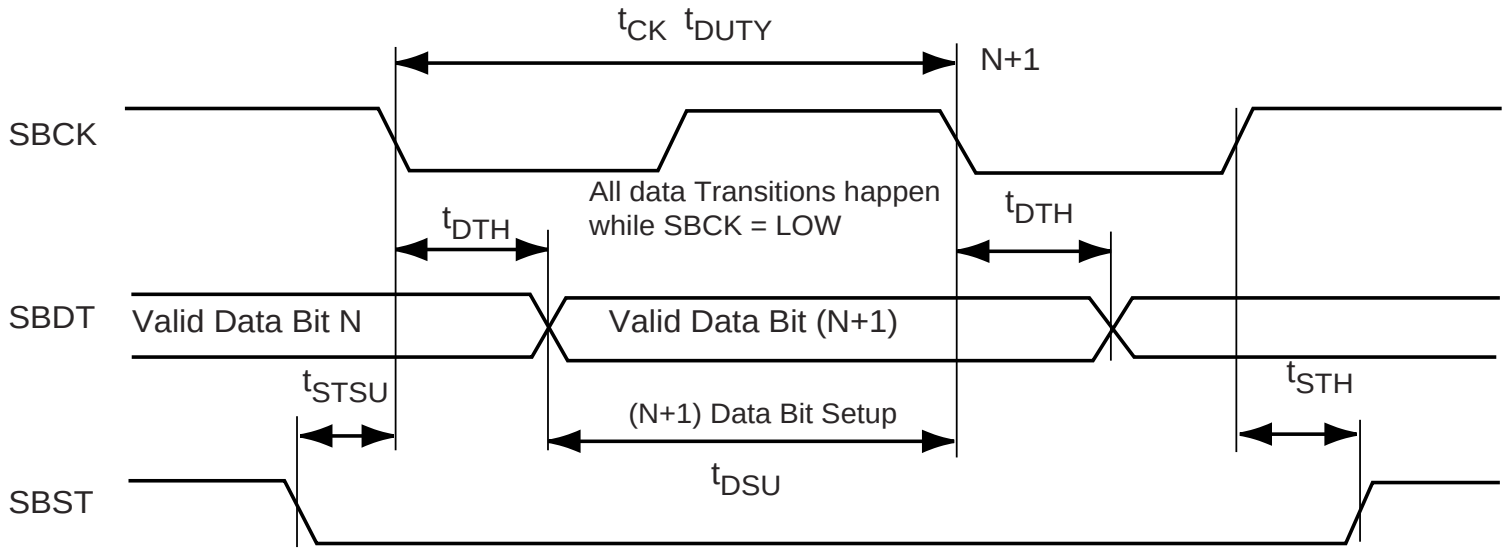


Figure 3: SBI Timing

Table 1 : SBI Bus Timing

Parameter	Description	Min	Max	Units
t_{CK}	SBCK period	0.6	10	µs
t_{DUTY}	SBCK duty cycle	35	65	%
t_{DSU}	SBDT setup time	$0.5 \bullet t_{CK} - t_{DTH}$	—	ns
t_{DTH}	SBDT hold time	—	$0.5 \bullet t_{SBI\_CLK\_SRC}$ [a]	ns
t_{STSU}	SBST setup time	50		ns
t_{STH}	SBST hold time	50	$0.5 \bullet t_{CK} - 100$	ns

[a] $t_{SBI\_CLK\_SRC}$ is the internal clock to the MSM Master SBI, which is selectable by MSM_CLK_CTL10.