7544 Group
Clock Synchronous Serial I/O

1. Abstract

The following article introduces and shows an application example of clock synchronous of serial I/O.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: 7544 Group

3. Contents

For clock synchronous serial I/O, the transmitter and the receiver use the same clock. Synchronizing with this clock, the transmit operation of the transmitter and the receive operation of the receiver are executed at the same time. If an internal clock is used as the operation clock, transfer is started by a write signal to the TB/RB.

3.1 Data Transfer Rate

The synchronous clock frequency is calculated by the following formula;

● When the internal clock is selected (when baud rate generator is used)

$$\text{Synchronous clock frequency [Hz]} = \frac{f(X_{IN})}{\text{Division ratio }^{*1} \times (\text{BRG setting value }^{*2} + 1) \times 4}$$

Division ratio[*1] : "1" or "4" is selected (set by bit 0 of serial I/O control register)
BRG setting value[*2] : 0 to 255 (00_{16} to FF_{16}) is set

● When the external clock is selected

$$\text{Synchronous clock frequency [Hz]} = \text{Clock input to } S_{CLK} \text{ pin}$$

3.2 Clock Synchronous Serial I/O Setting Method

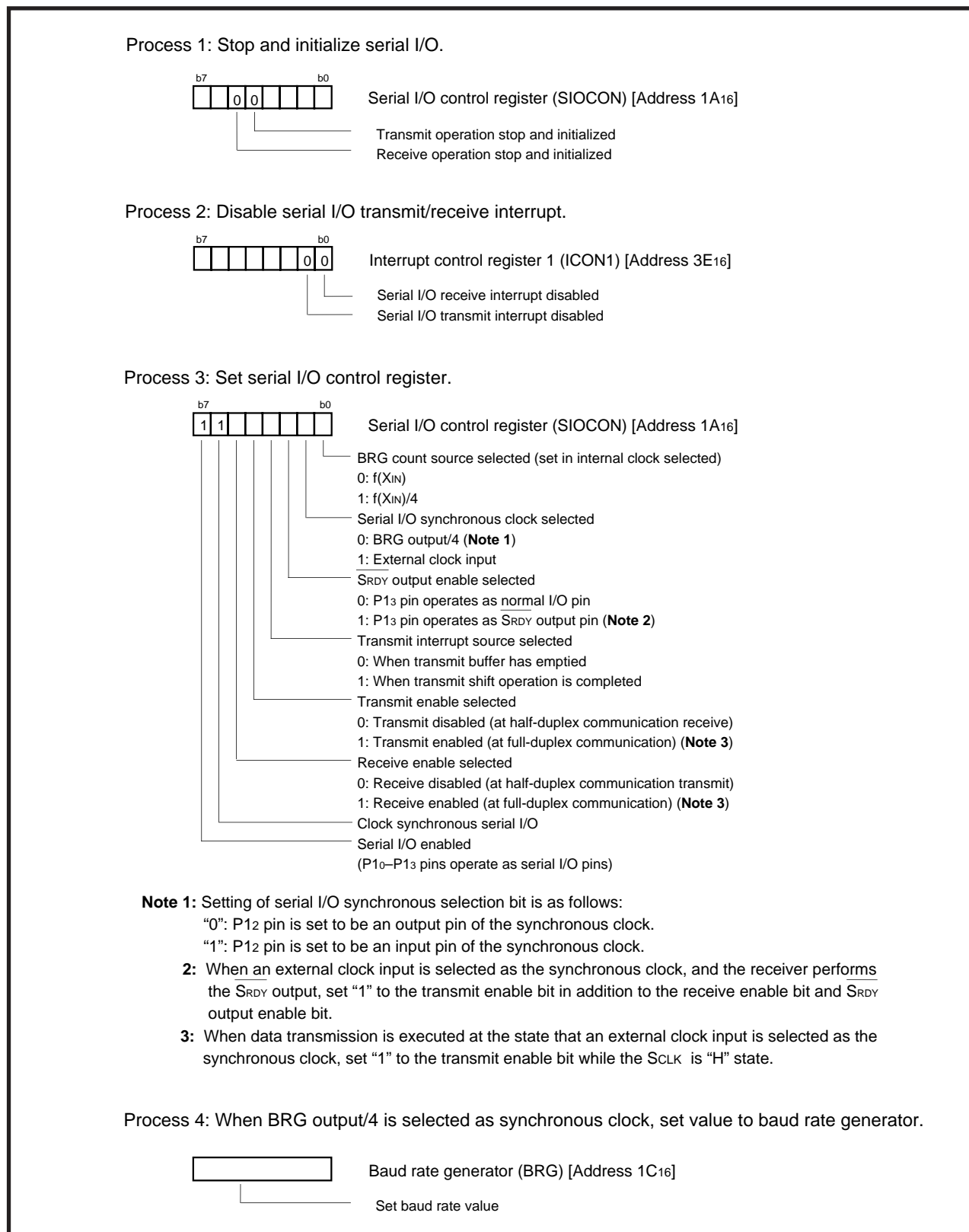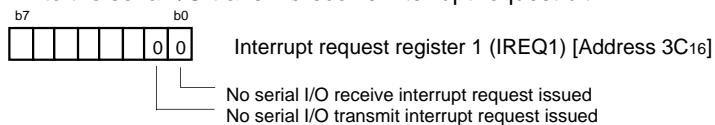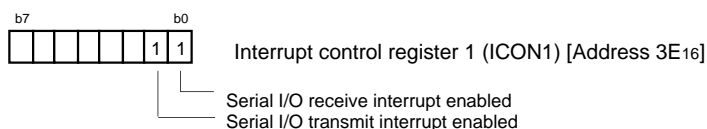Figure 1 and Figure 2 show the setting method for the clock synchronous serial I/O.

Process 1: Stop and initialize serial I/O.

b7   b0

| | 0 | 0 | | | | Serial I/O control register (SIOCON) [Address $1A_{16}$]

Transmit operation stop and initialized
Receive operation stop and initialized

Process 2: Disable serial I/O transmit/receive interrupt.

b7   b0

| | | | | | 0 | 0 | Interrupt control register 1 (ICON1) [Address $3E_{16}$]

Serial I/O receive interrupt disabled
Serial I/O transmit interrupt disabled

Process 3: Set serial I/O control register.

b7   b0

| 1 | 1 | | | | | | Serial I/O control register (SIOCON) [Address $1A_{16}$]

BRG count source selected (set in internal clock selected)
0: $f(X_{IN})$
1: $f(X_{IN})/4$
Serial I/O synchronous clock selected
0: BRG output/4 (**Note 1**)
1: External clock input
$\overline{S_{RDY}}$ output enable selected
0: P1₃ pin operates as normal I/O pin
1: P1₃ pin operates as $\overline{S_{RDY}}$ output pin (**Note 2**)
Transmit interrupt source selected
0: When transmit buffer has emptied
1: When transmit shift operation is completed
Transmit enable selected
0: Transmit disabled (at half-duplex communication receive)
1: Transmit enabled (at full-duplex communication) (**Note 3**)
Receive enable selected
0: Receive disabled (at half-duplex communication transmit)
1: Receive enabled (at full-duplex communication) (**Note 3**)
Clock synchronous serial I/O
Serial I/O enabled
(P1₀–P1₃ pins operate as serial I/O pins)

Note 1: Setting of serial I/O synchronous selection bit is as follows:
"0": P1₂ pin is set to be an output pin of the synchronous clock.
"1": P1₂ pin is set to be an input pin of the synchronous clock.
2: When an external clock input is selected as the synchronous clock, and the receiver performs the $\overline{S_{RDY}}$ output, set "1" to the transmit enable bit in addition to the receive enable bit and $\overline{S_{RDY}}$ output enable bit.
3: When data transmission is executed at the state that an external clock input is selected as the synchronous clock, set "1" to the transmit enable bit while the S_{CLK} is "H" state.

Process 4: When BRG output/4 is selected as synchronous clock, set value to baud rate generator.

| | | Baud rate generator (BRG) [Address $1C_{16}$]

Set baud rate value

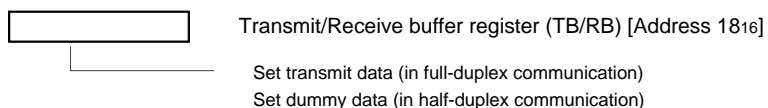**Figure 1 Setting method for clock synchronous serial I/O (1)**

Process 5: In order not to execute the no requested interrupt processing, set "0" (no requested)
to the serial I/O transmit/receive interrupt request bit.

b7   b0

| | | | | | | 0 | 0 | Interrupt request register 1 (IREQ1) [Address $3C_{16}$]

No serial I/O receive interrupt request issued
No serial I/O transmit interrupt request issued

Process 6: When the interrupt is used, set "1" (interrupt enabled) to the serial I/O transmit/receive
interrupt enable bit.

b7   b0

| | | | | | | 1 | 1 | Interrupt control register 1 (ICON1) [Address $3E_{16}$]

Serial I/O receive interrupt enabled
Serial I/O transmit interrupt enabled

Process 7: Transmit/Receive of serial data (**Notes 1, 2**).

Transmit/Receive buffer register (TB/RB) [Address 18_{16}]

Set transmit data (in full-duplex communication)
Set dummy data (in half-duplex communication)

Notes 1: When data transmission is executed at the state that an external clock input is
selected as the synchronous clock, set the transmit data while the S_{CLK} is "H" state.
2: When inputting the S_{RDY} signal, set used pins to to the input mode before
transmitting data.

Figure 2 Setting method for clock synchronous serial I/O (2)

3.3 Communication Using Clock Synchronous Serial I/O (Transmit/Receive)

Outline : 2-byte data is transmitted and received, using the clock synchronous serial I/O. $\overline{S_{RDY}}$ signal is used for communication control.

Specifications : •The serial I/O (clock synchronous serial I/O selected) is used.
•Synchronous clock frequency : 125 kHz; $f(X_{IN})$ = 4 MHz divided by 32
•The receiver outputs the $\overline{S_{RDY}}$ signal at 2 ms intervals which the timer generates, and 2-byte data is transferred from the transmitter to the receiver.

Figure 3 shows a connection diagram, Figure 4 shows a timing chart, Figure 5 shows the control procedure of transmitter, and Figure 6 shows an example of control procedure of receiver.
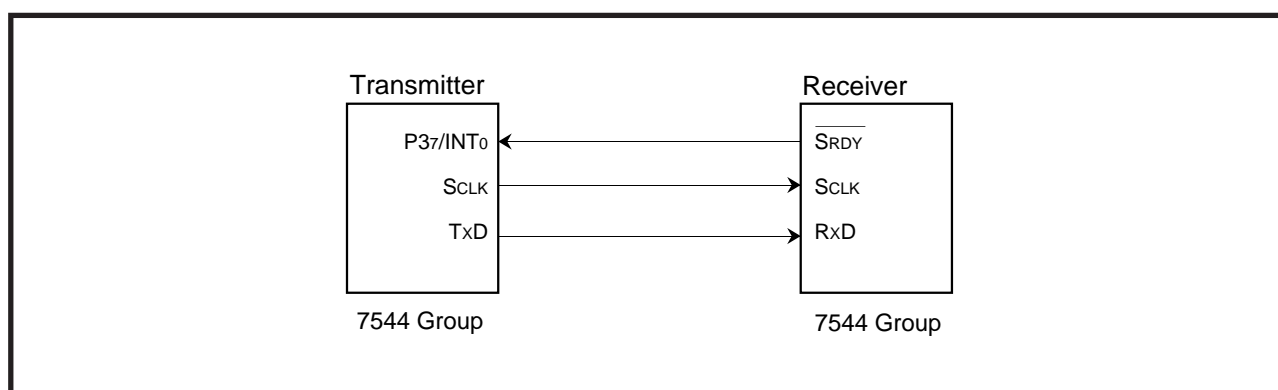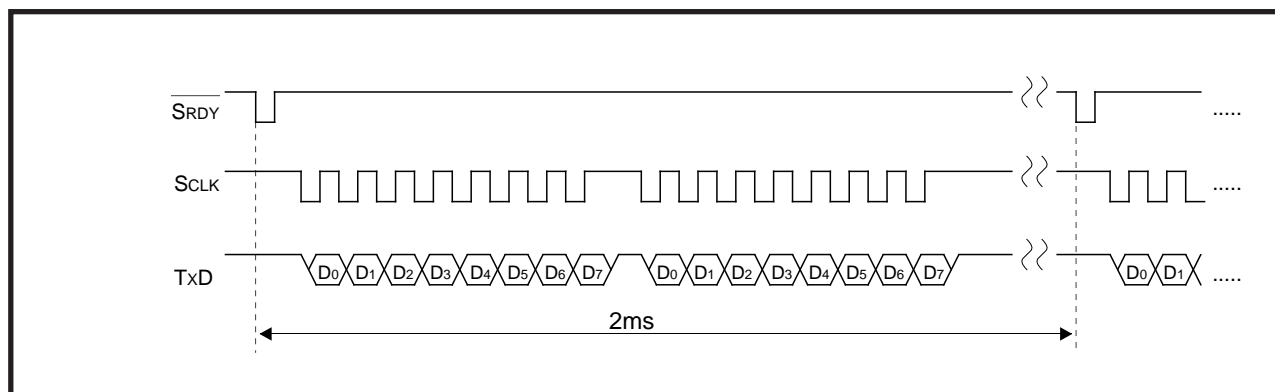

Figure 3 Connection diagram
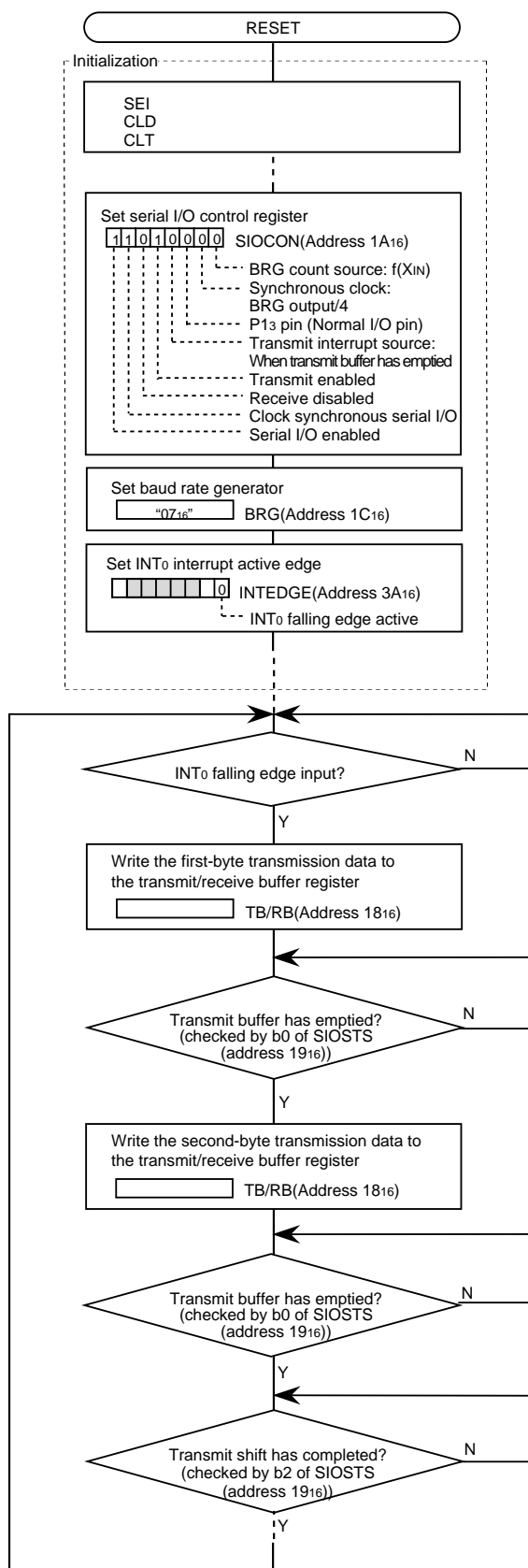

Figure 4 Timing chart

RESET

Initialization

SEI
CLD
CLT

Set serial I/O control register

1 1 0 1 0 0 0 0 SIOCON(Address 1A16)

BRG count source: f(XIN)
Synchronous clock:
BRG output/4
P13 pin (Normal I/O pin)
Transmit interrupt source:
When transmit buffer has emptied
Transmit enabled
Receive disabled
Clock synchronous serial I/O
Serial I/O enabled

Set baud rate generator

"0716" BRG(Address 1C16)

Set INT0 interrupt active edge

0 INTEDGE(Address 3A16)

INT0 falling edge active

INT0 falling edge input? — N

Y

Write the first-byte transmission data to
the transmit/receive buffer register

TB/RB(Address 1816)

Transmit buffer has emptied?
(checked by b0 of SIOSTS
(address 1916)) — N

Y

Write the second-byte transmission data to
the transmit/receive buffer register

TB/RB(Address 1816)

Transmit buffer has emptied?
(checked by b0 of SIOSTS
(address 1916)) — N

Y

Transmit shift has completed?
(checked by b2 of SIOSTS
(address 1916)) — N

Y

Figure 5 Control procedure of transmitter
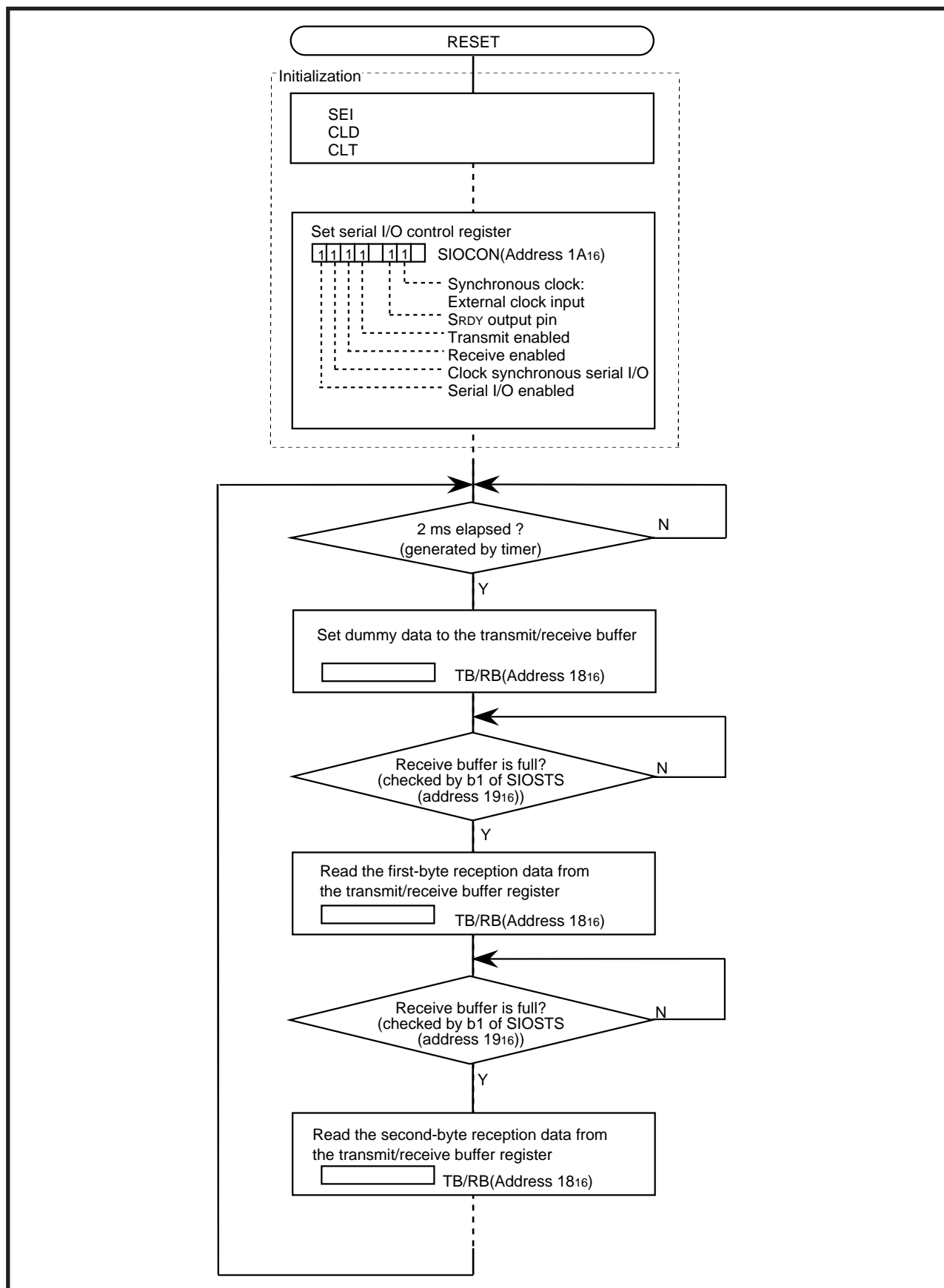
Figure 6 Control procedure of receiver

The flowchart contains the following elements:

RESET

Initialization:

SEI
CLD
CLT

Set serial I/O control register
1 1 1 1 1 1   SIOCON(Address 1A₁₆)
Synchronous clock:
External clock input
S$_{RDY}$ output pin
Transmit enabled
Receive enabled
Clock synchronous serial I/O
Serial I/O enabled

2 ms elapsed ?
(generated by timer)   N

Y

Set dummy data to the transmit/receive buffer
TB/RB(Address 18₁₆)

Receive buffer is full?
(checked by b1 of SIOSTS
(address 19₁₆))   N

Y

Read the first-byte reception data from
the transmit/receive buffer register
TB/RB(Address 18₁₆)

Receive buffer is full?
(checked by b1 of SIOSTS
(address 19₁₆))   N

Y

Read the second-byte reception data from
the transmit/receive buffer register
TB/RB(Address 18₁₆)

4. Sample Programming Code

```
[Reset Start ••• Main Routine Process]

RESET:
        SEI                         ; Interrupt disable
        CLD
        CLT
;
        LDX  #$FF                   ; Set stack bottom
        TXS
;
        LDM  #%10000000,CPUM        ; Set CPU mode register
;
; Wait f(XIN) oscillation stabilizing time
;
        LDM  #%00000000,CPUM        ; Set CPU mode register
;
        LDA  #0
        LDX  #>RAM_top
RAM_clear:STA $00,X
        INX
        BNE  RAM_clear
;
Sio_initial:
        LDM  #%11010000,SIOCON      ; BRG count source : f(Xin)
                                    ; synchronous clock : divided 4
                                    ; P1_3 function : normal I/O pin
                                    ; interrupt request factor : transmit buffer is empty
                                    ; enable transmit
                                    ; disable receive
                                    ; serial I/O mode : synchronous serial I/O mode
                                    ; enable serial I/O
        LDM  #$07,BRG               ; set baud rate

        CLB  0,INTEDGE              ; INT0 falling edge active

        LDM  #$055,SEND_DATA
        LDM  #$0AA,SEND_DATA+1

;
;
;--------------------------------------------------------------------------------
__MAIN:
        BBC  2,IREQ1,__MAIN         ; input INT0 falling edge
        CLB  2,IREQ1

        LDA  SEND_DATA
        STA  TBRB                   ; Send data write

__MAIN00:
        BBC  0,SIOSTS,__MAIN00      ; data send? -> no
;
        LDA  SEND_DATA+1
        STA  TBRB                   ; Next send data write

__MAIN01:
        BBC  0,SIOSTS,__MAIN01      ; data send? -> no
;
__MAIN02:
        BBC  2,SIOSTS,__MAIN02      ; Shift end check ? -> no
;
        BRA  __MAIN
;
```

Figure 7 Sample Programming Code (Transmit Side)

```
[Reset Start ••• Main Routine Process]

RESET:
            SEI                         ; Interrupt disable
            CLD
            CLT
;
            LDX   #$FF                   ; Set stack bottom
            TXS
;
            LDM   #%10000000,CPUM        ; Set CPU mode register
;
; Wait f(XIN) oscillation stabilizing time
;
            LDM   #%00000000,CPUM        ; Set CPU mode register
;
            LDA   #0
            LDX   #>RAM_top
RAM_clear:  STA   $00,X
            INX
            BNE   RAM_clear
;
Sio_initial:
            LDM   #%11110110,SIOCON     ; synchronous clock : external clock
                                        ; P1_3 pin function : SRDY output pin
                                        ; enable transmit
                                        ; enable receive
                                        ; serial I/O mode : synchronous serial I/O mode
                                        ; enable serial I/O

            LDM   #$00,TCSS2            ; select timer 1 count source : f(Xin)/16
            LDM   #65-1,PRE1            ; Set Prescaler 1
            LDM   #8-1,T1               ; Set Timer 1
            CLB   5,IREQ2               ; clear timer 1 interrupt request
            NOP

;
;----------------------------------------------------------------------------
__MAIN:
            BBC   5,IREQ2,__MAIN        ; 2ms?
            CLB   5,IREQ2

            LDA   #$00                  ; write dummy data
            STA   TBRB

__MAIN_00:
            BBC   1,SIOSTS,__MAIN_00    ; data receive ? -> no
;
            LDA   TBRB
            STA   Receive_Data          ; store receive data

            LDA   #$00                  ; write dummy data
            STA   TBRB

__MAIN01:
            BBC   1,SIOSTS,__MAIN01     ; data receive ? -> no
;
            LDA   TBRB
            STA   Receive_Data+1        ; store next receive data

            BRA   __MAIN
;
```

Figure 8 Sample Programming Code (Receive Side)

5. Reference

Data Sheet
7544 Group Data sheet
7544 Group Data sheet (QzROM Version)

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		Page	Summary
1.00	Apr 01, 2003	-	First Edition issued
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