BASIC PIC16/17 OSCILLATOR DESIGN

By: Dan Matthews

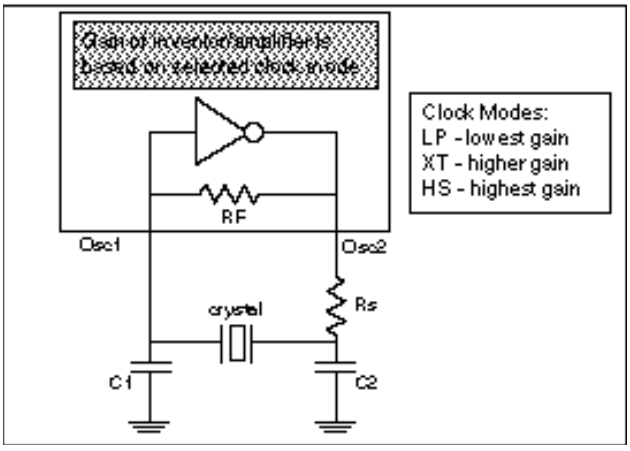
The oscillator circuit is one of the most overlooked areas of microprocessor circuit design. Components are usually selected based on the manufacturers' tables. If the circuit starts up and works, fine, no other thought need be given to it, right? Wrong. Many conditions can negatively affect the performance of your design. Higher temperatures and lower supply voltages can lower the loop gain in the oscillator circuit, causing poor, slow, or no startup. Colder temperatures and higher supply voltages can increase the loop gain of the oscillator circuit, causing the crystal to be overdriven, and potentially damaged; or the circuit can be forced to another harmonic and throw off the timing or cease functioning altogether. It is also possible to waste power through the improper selection of components or clock modes.

Most of the time using the values given in the manufacturers' databook tables will work fine. However, most manufacturers' processors run in a limited voltage range and across a limited frequency, so table values can be given for C1 and C2 with little concern for the designer's environment. Microchip parts, however, can be asked to run with clocks from 0 to 25 MHz, supply voltages from 2.0VDC to 6.25VDC, and temperatures from -40°C to 125°C, depending on the part and version ordered. This must also be done with crystals of varying quality and manufacture. These factors create many chances for exceptions to the values given in the databook.

Function of the Oscillator Circuit

The circuit (Figure 1) is a typical Pierce parallel resonant oscillator circuit as used with the Microchip PIC16/17 family of devices. The output of an inverting amplifier is fed back to its input creating an "unstable" loop. When the inverter output is high and fed back to the input, output goes low, reversing the process. Stable oscillation is achieved when the circuit components attached achieve this feedback with "unity gain" only at the desired frequency.

FIGURE 1: TYPICAL PIERCE PARALLEL RESONANT OSCILLATOR CIRCUIT



Purpose of Components and Clock Modes

A good place to begin is with the purpose of each external component. Because this is a loop circuit a change in one component can change the affect of other components in the circuit. Therefore, a strict definition of purpose is a simplification for clarity only.

The Crystal has its lowest impedance near the desired frequency. This is placed in the path between the output and the input of the inverting amplifier. This permits feedback, and therefore oscillation, which occurs at the desired resonant frequency.

The diagrams shown below illustrate an equivalent circuit for a crystal (Figure 2), and the impedance/reactance versus frequency of the crystal (Figure 3). Cc represents the case capacitance across the terminals of the crystal. R, Cp, and Lp are known as the motional arm of the crystal. In parallel resonant mode (Anti-resonance) the crystal will look inductive to the circuit. The impedance will reache its peak at fa. The load capacity should be selected to operate the crystal at a stable point on the fs-fa reactive curve (as close to fs as possible).

Note:	Even parallel resonant crystals have a series resonant frequency fs.

FIGURE 2: EQUIVALENT CRYSTAL CIRCUIT

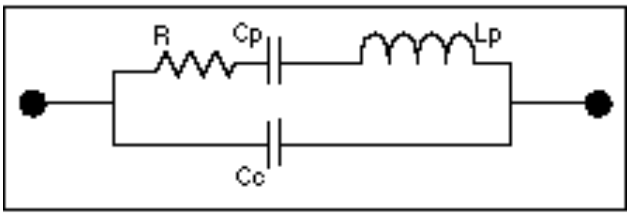
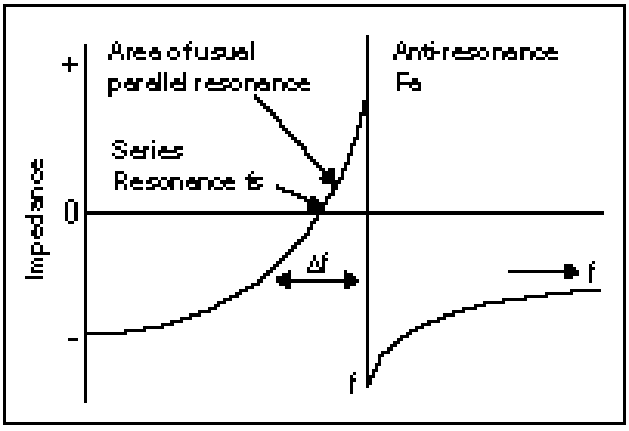


FIGURE 3: IMPEDANCE/REACTANCE vs CRYSTAL FREQUENCY



C1 of Figure 1 is a "phase adjusting" capacitor. It also contributes slightly to start up time and is part of the load capacitance for a parallel resonant circuit. Phase is affected since C1 is at the clock input pin and charged through the impedance of the crystal.

C2 is a "gain adjusting" capacitor. Selected for best sinusoidal output voltage peak to peak. It is also part of the load capacitance for a parallel resonant circuit.

Load capacitance for a parallel resonant circuit can be calculated by: $\frac{C1 \times C2}{C1 + C2} + Cstray$

and should be selected per the data supplied by the crystal manufacture.

Cstray in the above equation can be pin capacitance and board/trace related capacitance. This is often seen in the ballpark of 5-15 pF. If the Microchip databook shows 15 pF capacitors for C1 and C2, and your board and device have 12.5 pF Cstray, then the resulting load capacitance in pF is [(15 * 15)/(15 + 15)] + 12.5 = 20 pF. If the crystal manufacturer suggests a load capacitance of 20 pF, then voila, you're there. If you decide to increase C2 to 33 pF (see "Selecting Best Values..." and "Start Up"), the resulting load capacitance is still 22.8 pF. In most cases deviations greater than this will not "pull" the resulting resonant frequency appreciably.

Rs is a series resistor that is selected to prevent overdriving the crystal. It is often not needed if gain (clock mode), C1 and C2 are selected properly.

Clock Mode is the programmable gain of the inverting amplifier. The lower frequency modes have lower gain, the gain increases for higher frequency modes. For instance, in the PIC16CXXX family, the clock mode gain from lowest to highest is LP (lowest gain), XT (middle), and HS (highest gain).

Selection of Components

There are several factors that go into the selection and arrangement of these external components. Some of these are amplifier gain, desired frequency and the resonant frequency(s) of the crystal, temperature of operation, supply voltage and its range, start up time, stability, crystal life, power consumption, simplification of the circuit and use of standard components (as few as possible). To say that there are a lot of factors, and that there are trade-offs with each, is an understatement.

Determining Best Values for Clock Mode, C1, C2 and Rs

The best method for selecting components is a little knowledge and a lot of trial, measurement and testing.

Crystals are usually selected by their parallel resonant frequency only, however, other parameters may be important to your design such as temperature or frequency tolerance. Application Note 588 is an excellent reference if you would like to know more about crystal operation and their ordering information.

The Microchip devices utilize a parallel oscillator circuit which requires that a parallel resonant crystal be selected. The load capacitance is usually specified in the 20 pF to 32 pF range. The crystal will oscillate closest to the desired frequency when this load capacitance is used. It is necessary sometimes to juggle these values a bit, as I will describe later, in order to achieve other benefits.

Clock mode is primarily chosen by using the table found in the Microchip databook based on frequency. Clock modes (except RC) are simply gain selections: lower gain for lower frequencies and higher gain for higher frequencies. It is possible to select a higher or lower gain if desired based on the specific needs of the oscillator circuit. In circuits where low power consumption is critical, a lower gain clock mode can help. The trade-offs are that lower gain can increase start up time and it is difficult to get the needed loop gain at higher frequencies if a lower gain clock mode is chosen. Higher gain clock modes are normally chosen for higher frequencies and improved start up time. The trade offs for higher gain are increased power consumption and the potential to design an unstable circuit, or overdrive the crystal, especially at low frequencies.

It is possible for a crystal to oscillate in a higher overtone frequency if the loop gain of the oscillator circuit is greater than one at that frequency. Depending on whether they are mechanical or electrical, overtones can come at 2X, 3X and odd multiples of the resonant frequency. Overdriving the crystal can cause break down or frequency drift (usually drifts up) over time. This can be handled through proper selection of C1, C2 and Rs.

Again, the mode listed in the databook for the desired frequency is the obvious starting point until you have some special reason to deviate from it. While clock mode can affect power consumption somewhat (higher gain / higher consumption), it is the frequency that the processor is running at that has by far the greatest impact on power consumption. Some designers have made the mistake of trying to run a part at high frequencies, say 8 MHz, while using the LP (low power) clock mode. Then they wonder why the processor doesn't start up sometimes. Running outside the recommended range for the clock mode should be avoided unless you understand the ramifications.

C1 and C2 should also be initially selected based on the load capacitance, as suggested by the crystal manufacturer, and the tables supplied in the Microchip databook. The values given in the Microchip databook can only be used as a starting point since the manufacturer of the crystal, supply voltage and other factors already mentioned may cause your circuit to differ from the one used in the factory characterization process.

Ideally, the lowest capacitance is chosen (within the range of the recommended crystal load preferably) that will oscillate at the highest temperature and lowest V_{DD} that the circuit will be expected to perform under. High temperature and low V_{DD} both have a limiting affect on the loop gain, such that if the circuit functions at these extremes the designer can be more assured of proper operation at other temperatures and supply voltages. Another method for improving start up is to use a value of C2 greater than C1. This causes a greater phase shift across the crystal at power up which speeds oscillator start up.

Besides loading the crystal for proper frequency response, these capacitors can also have the affect of lowering loop gain if their value is increased. C2 can be selected to affect the overall gain of the circuit. A higher C2 can lower the gain if the crystal is being over driven. (See also discussion on Rs.) C values that are too high can store and dump too much current through the crystal so C1 and C2 should not become excessively large. Unfortunately, measuring the wattage through a crystal is tricky business, but if you do not stray too far from the suggested values you should not have to be concerned with this.

Rs is selected if, after all other devices are selected to satisfaction, the crystal is still being overdriven. This can be determined by looking at the osc-out pin, which is the driven pin, with an oscilloscope. Connecting the probe to the osc-in pin will load the pin too much and negatively affect performance. Remember that a scope probe adds its own capacitance to the circuit so this may have to be accounted for in your design (i.e., if the circuit worked best with a C2 of 20 pF and scope probe was 10 pF, a 30 pF capacitor may actually be called for). The output signal should not be clipping or squashed. Overdriving the crystal can also lead to the circuit jumping to a higher harmonic.

The osc-out signal should be a nice clean sine wave that easily spans the input minimum and maximum of the clock input pin (4.25V to 5.0V peak to peak for a 5.0V V_{DD} is usually good). An easy way to set this is to again test the circuit at minimum temperature and maximum V_{DD} that the design will be expected to perform in, then look at the output. This should be the maximum amplitude of the clock output. If there is clipping or the sine wave is squashing near V_{DD} and V_{SS} at the top and bottom, and increasing load capacitors will risk too much current through the crystal or push the value too far from the manufacturer's load specification, then add a trimpot between the output pin and C2 and adjust it until the sine wave is clean. Keeping it fairly close to maximum amplitude at this low temperature and high V_{DD} combination will assure that this is the maximum amplitude the crystal will see and prevent overdriving. An Rs of the closest standard value can now be inserted in place of the trimpot. If Rs is too high, perhaps more than 5 kW, the input will be too isolated from the output, making the clock more susceptible to noise. If you find a value this high is needed to prevent overdriving the crystal, try increasing C2 to compensate. Try to get a combination where Rs is around 1K or less, and load capacitance is not too far from the 20 pF or 32 pF manufacturer specification.

Start Up

The most difficult time for the oscillator to start up is waking up from sleep. This is because the load capacitors have partially charged to some quiescent value and phase differential at wake up is minimal. Thus, more time is required for stable oscillation. Remember also that low voltage, high temperatures and lower frequency clock modes also impose limitations on loop gain which in turn affects start up. The worst possible case is a low frequency design (with its low gain clock mode), in a quiet environment (like a battery operated device), operating outside noisy RF area of the city (or in a shielded box), with a low battery, on a hot day, waking up from sleep.

There is an old designer's tip, though I have not proven it for myself, that a cheap Rs resistor, such as a carbon film or carbon composition resistor, can actually help start oscillation. An oscillator circuit depends on some stray noise to start up. Usually the power up process will provide this, but if the processor is put to sleep, the oscillator will have to start up on wake up without the power up ramp (although some noise is created internally by the wake up logic). Cheap carbon resistors generate some amount of white noise which when placed in the crystal oscillator path can assist start up.

Remember that C2 can be increased over C1 to increase phase shift and help start up, especially at lower frequencies. Another possibility is to select a higher gain clock mode. For instance, if start up is a concern for a device running at a frequency that would normally be the LP mode range, XT mode can be selected. Usually this is a last resort since the other suggestions already mentioned have been proven to work and using a higher gain mode introduces increased potential for overdriving the crystal. The higher gain creates a faster higher drive start up edge that can help reduce start up time. C2 may have to be increased, and/or a Rs added to prevent overdriving the crystal.

It is also possible for a circuit with too much gain to not start up. This usually happens when using a low frequency crystal, like 32 kHz, since at high frequencies the high gain is dissipated more easily by the load capacitance. Because of great customer demand for a fast start up processor, even at low frequencies, Microchip has increased the gain of the LP mode for newer devices. This may require higher capacitance values or a Rs. For instance, for the PIC16C71, the capacitance values of 15 pF on each pin, as suggested by the databook for 32 kHz, is not always sufficient. Increasing the values to 22 pF or 33 pF for C1 and 33 pF or 47 pF for C2 usually fixes this. Again, if you desire that the circuit oscillate at the resonant frequency to be as accurate as possible, you may be better served by adding a Rs to the circuit as needed and keep the capacitor values closer to the load capacitance suggested by the crystal manufacturer. Refer to the Rs section of this article for details on determining the Rs value.

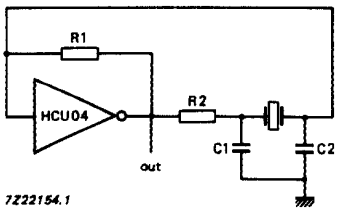
The Final Check

Remember, check that the output sine wave is not clipping in the highest gain environment of highest V_{DD} and lowest temperature. Also make sure that the sine output amplitude is great enough, in the lowest gain environment of lowest V_{DD} and highest temperature, to cover the logic input requirements of the clock as listed in the device datasheet. 4.25V peak to peak is usually fine. Then at the highest temperature with the lowest V_{DD} it will have to run at, running from a quiet battery if possible and in as quiet an environment as your board will see (RF and electrically speaking), test the part to make sure it wakes up from sleep. If all this checks out and your capacitance values are low enough, within range to prevent unnecessary power consumption, then you should have a clean trouble free oscillator design.

A Note on External Clocks

If the PIC16/17 internal oscillator is not being used, and the device will be driven from an external clock, be sure to set the clock mode to something other than RC mode (RC mode will fight with the injected input). Ideally you would select the mode that corresponds to the frequency injected. This is of less importance here since the clock is only driving its internal logic and not a crystal loop circuit. It may be possible to select a clock mode lower than would be needed by an oscillator circuit, thereby saving some of the power that would beused to exercise the inverting amplifier. Make sure the osc-out signal amplitude covers the needed logic thresholds of the device.

For really power stingy applications, with high speed external clocks approaching 20 MHz, the device will draw less power if the clock is injected at the osc-out pin. This can only be done with devices where the internal logic is driven from osc-out. A diagram of the clock circuitry is provided in the databook for each device. If the frequency is high enough, the internal capacitance and impedances will serve to isolate the internal inverter output from the signal enough so that it will not challenge the injected signal. The internal feedback resistor is weak enough to allow the inverter to find a quiescent point. Since the inverter is not being exercised, less power is drawn. Again, this is operating outside the normal design criteria so you should be extremely thorough in testing and proving your design before calling it complete.

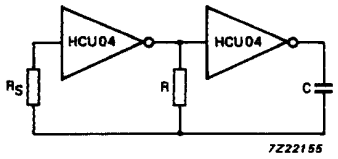


C_1 = 47 pF (typ.)
C_2 = 33 pF (typ.)
R_1 = 1 to 10 MΩ (typ.)

R_2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 5 mA at V_{CC} = 5 V and f = 10 MHz).

Fig.13 Crystal oscillator configuration.

$$f = \frac{1}{T} \approx \frac{1}{2.2\ RC}$$



$R_S \approx 2 \times R$.

The average I_{CC} (mA) is approximately
$3.5 + 0.05 \times f\ (MHz) \times C\ (pF)$ at V_{CC} = 5.0 V
(for more information refer to *"DESIGNERS GUIDE"*).

Fig.14 HCU04 used as an astable multivibrator

OPTIMUM VALUE FOR R_2

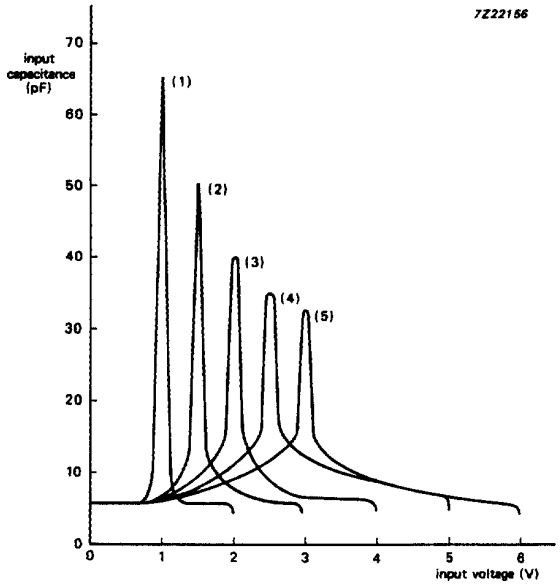
FREQUENCY (MHz)	R_2 (kΩ)	OPTIMUM FOR
3	2 8	minimum required I_{CC} minimum influence due to change in V_{CC}
6	1 4.7	minimum I_{CC} minimum influence by V_{CC}
10	0.5 2	minimum I_{CC} minimum influence by V_{CC}
14	0.5 1	minimum I_{CC} minimum influence by V_{CC}
> 14	replace R_2 by C_3 with a typical value of 35 pF	

EXTERNAL COMPONENTS FOR RESONATOR (f < 1 MHz)

FREQUENCY (kHz)	R_1 (MΩ)	R_2 (kΩ)	C_1 (pF)	C_2 (pF)
10 to 15.9	22	220	56	20
16 to 24.9	22	220	56	10
25 to 54.9	22	100	56	10
55 to 129.9	22	100	47	5
130 to 199.9	22	47	47	5
200 to 349.9	10	47	47	5
350 to 600	10	47	47	5

Note

1. All values given are typical and must be used as an initial set-up.



(1) V_{CC} = 2.0 V.
(2) V_{CC} = 3.0 V.
(3) V_{CC} = 4.0 V.
(4) V_{CC} = 5.0 V.
(5) V_{CC} = 6.0 V.

Fig.15 Typical input capacitance as a function of input voltage.

Note to Application information

All values given are typical unless otherwise specified.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.