

Power MOSFET Basics -- Vrej Barkhordarian, International Rectifier, El Segundo, Ca.

Introduction to Power MOSFETs and their Applications -- Fairchild Semiconductor

Understanding Power MOSFETs -- Fairchild Semiconductor

The Do's and Don'ts of Using MOS-Gated Transistors -- International Rectifier

Current Ratings of Power Semiconductors -- International Rectifier

Gate Drive Characteristics and Requirements for HEXFETS -- International Rectifier

Mounting Considerations For IR's Power Semiconductor Packages -- International Rectifier

Mounting Guidelines for the SUPER-247 -- Andrew Sawle and Arthur Woodworth, IR

Calculating temperature gradients in power MOSFETS with "HEXRise" program -- International Rectifier

MOSFET Thermal Characterization in the Application -- Siliconix/Vishay

Power MOSFET Basics

Vrej Barkhordarian, International Rectifier, El Segundo, Ca.

<http://www.irf.com/technical-info/appnotes/mosfet.pdf>

Discrete power MOSFETs employ semiconductor processing techniques that are similar to those of today's VLSI circuits, although the device geometry, voltage and current levels are significantly different from the design used in VLSI devices. The metal oxide semiconductor field effect transistor (MOSFET) is based on the original field-effect transistor introduced in the 70s. Figure 1 shows the device schematic, transfer characteristics and device symbol for a MOSFET. The invention of the power MOSFET was partly driven by the limitations of bipolar power junction transistors (BJTs) which, until recently, was the device of choice in power electronics applications.

Although it is not possible to define absolutely the operating boundaries of a power device, we will loosely refer to the power device as any device that can switch at least 1A. The bipolar power transistor is a current controlled device. A large base drive current as high as one-fifth of the collector current is required to keep the device in the ON state.

Also, higher reverse base drive currents are required to obtain fast turn-off. Despite the very advanced state of manufacturability and lower costs of BJTs, these limitations have made the base drive circuit design more complicated and hence more expensive than the power MOSFET.

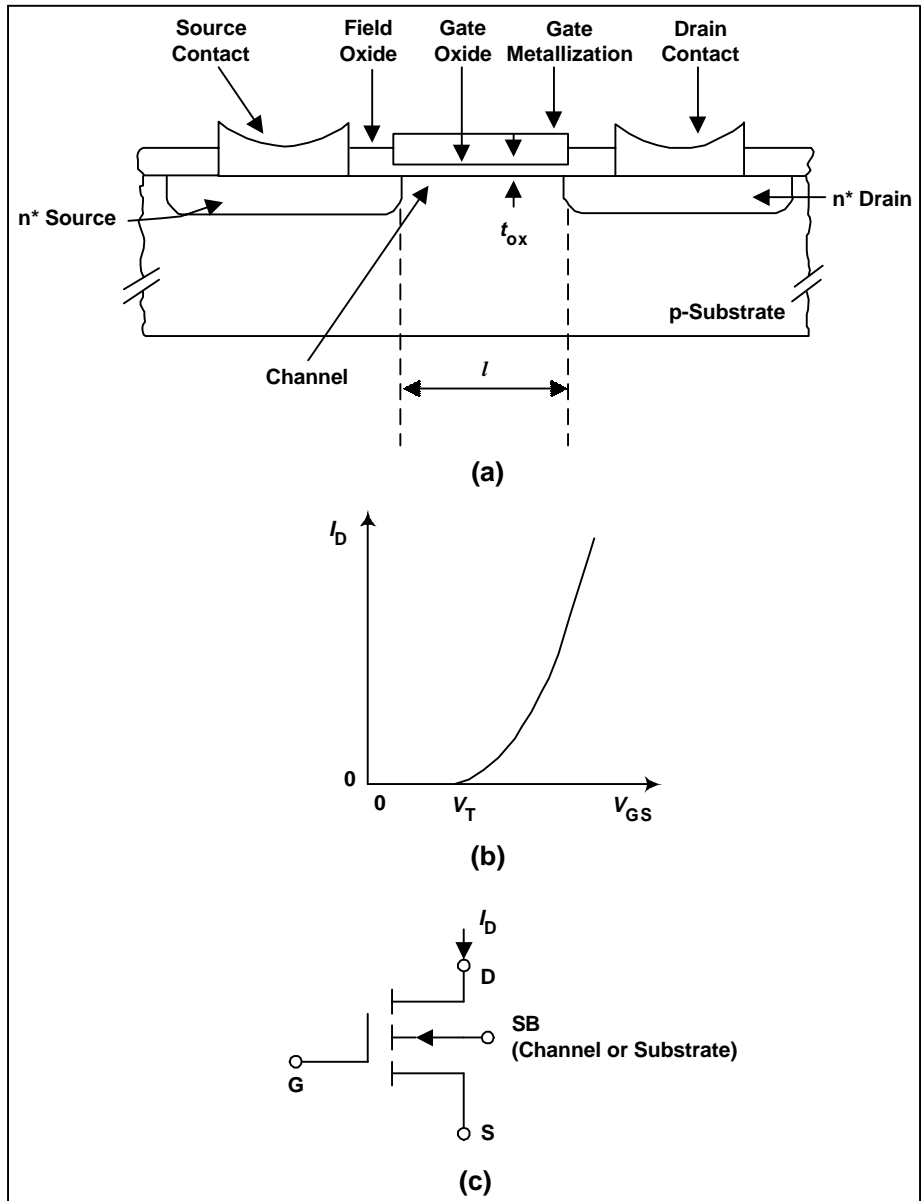


Figure 1. Power MOSFET (a) Schematic, (b) Transfer Characteristics, (c) Device Symbol.

Another BJT limitation is that both electrons and holes contribute to conduction. Presence of holes with their higher carrier lifetime causes the switching speed to be several orders of magnitude slower than for a power MOSFET of similar size and voltage rating. Also, BJTs suffer from thermal runaway. Their forward voltage drop decreases with increasing temperature causing diversion of current to a single device when several devices are paralleled. Power MOSFETs, on the other hand, are majority carrier devices with no minority carrier injection. They are superior to the BJTs in high frequency applications where switching power losses are important. Plus, they can withstand simultaneous application of high current and voltage without undergoing destructive failure due to second breakdown. Power MOSFETs can also be paralleled easily because the forward voltage drop increases with increasing temperature, ensuring an even distribution of current among all components.

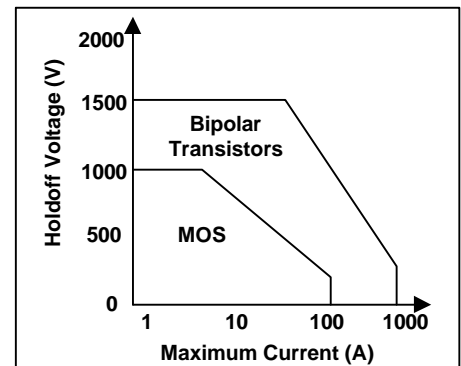


Figure 2. Current-Voltage Limitations of MOSFETs and BJTs.

However, at high breakdown voltages (>200V) the on-state voltage drop of the power MOSFET becomes higher than that of a similar size bipolar device with similar voltage rating. This makes it more attractive to use the bipolar power transistor at the expense of worse high frequency performance. Figure 2 shows the present current-voltage limitations of power MOSFETs and BJTs. Over time, new materials, structures and processing techniques are expected to raise these limits.

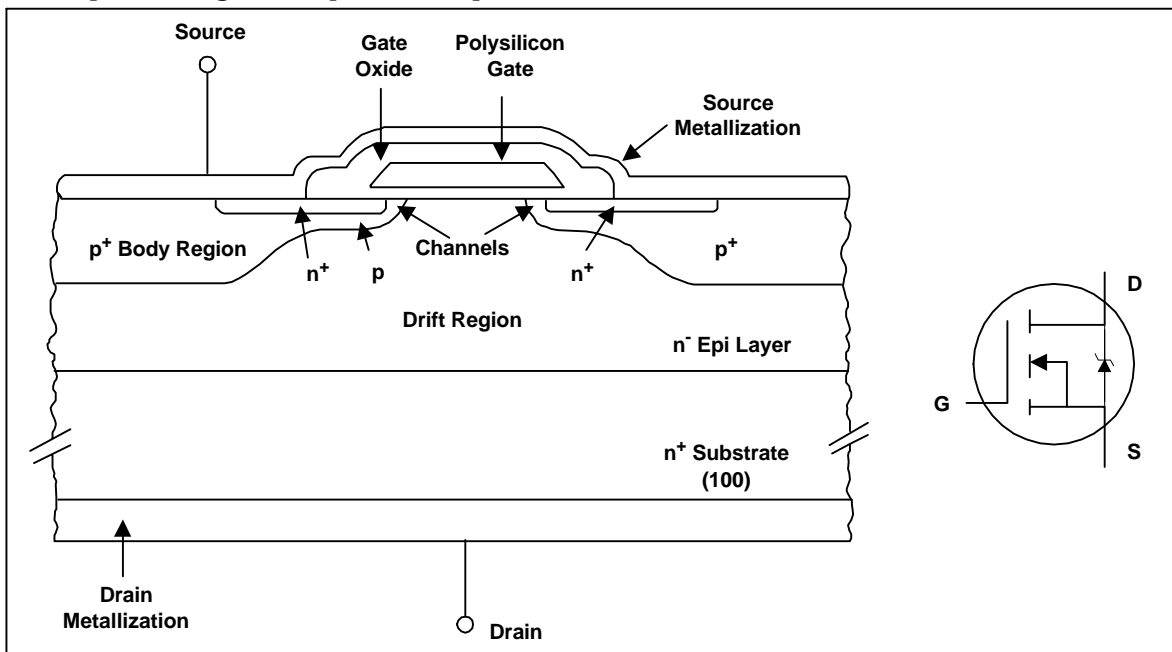


Figure 3. Schematic Diagram for an n-Channel Power MOSFET and the Device.

Figure 3 shows schematic diagram and Figure 4 shows the physical origin of the parasitic components in an n-channel power MOSFET. The parasitic JFET appearing between the two body implants restricts current flow when the depletion widths of the two adjacent body diodes extend into the drift region with increasing drain voltage. The parasitic BJT can make the device susceptible to unwanted device turn-on and premature breakdown. The base resistance R_B must be minimized through careful design of the doping and distance under the source region. There are several parasitic capacitances associated with the power MOSFET as shown in Figure 3.

C_{GS} is the capacitance due to the overlap of the source and the channel regions by the polysilicon gate and is independent of applied voltage. C_{GD} consists of two parts, the first is the capacitance associated with the overlap of the polysilicon gate and the silicon underneath in the JFET region. The second part is the capacitance associated with the depletion region immediately under the gate. C_{GD} is a nonlinear function of voltage. Finally, C_{DS} , the capacitance associated with the body-drift diode, varies inversely with the square root of the drain-source bias. There are currently two designs of power MOSFETs, usually referred to as the planar and the trench designs. The planar design has already been introduced in the schematic of Figure 3. Two variations of the trench power MOSFET are shown Figure 5. The trench technology has the advantage of higher cell density but is more difficult to manufacture than the planar device.

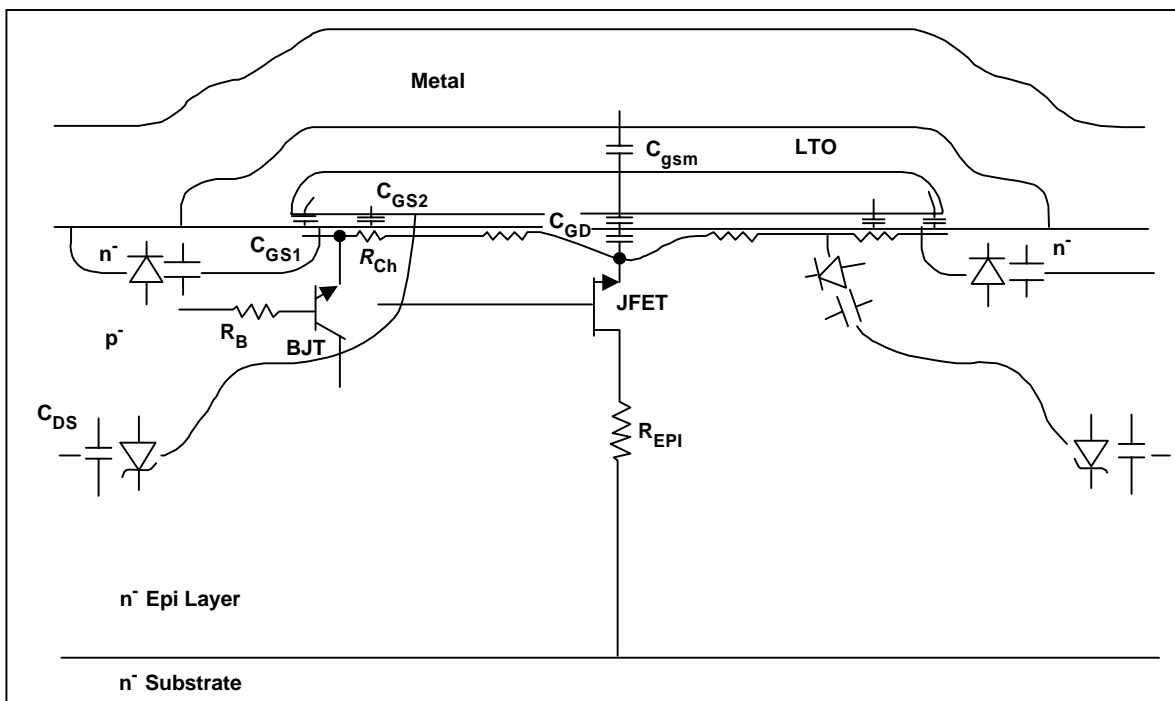


Figure 4. Power MOSFET Parasitic Components.

BREAKDOWN VOLTAGE

Breakdown voltage, BV_{DSS} , is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the source and drain by the avalanche multiplication process, while the gate and source are shorted together. Current-voltage characteristics of a power MOSFET are shown in Figure 6. BV_{DSS} is normally measured at $250\mu A$ drain current. For drain voltages below BV_{DSS} and with no bias on the gate, no channel is formed under the gate at the surface and the drain voltage is entirely supported by the reverse-biased body-drift p-n junction. Two related phenomena can occur in poorly designed and processed devices: punch-through and reach-through. Punch-through is observed when the depletion region on the source side of the body-drift p-n junction reaches the source region at drain voltages below the rated avalanche voltage of the device. This provides a current path between source and drain and causes a soft breakdown characteristics as shown in Figure 7. The leakage current flowing between

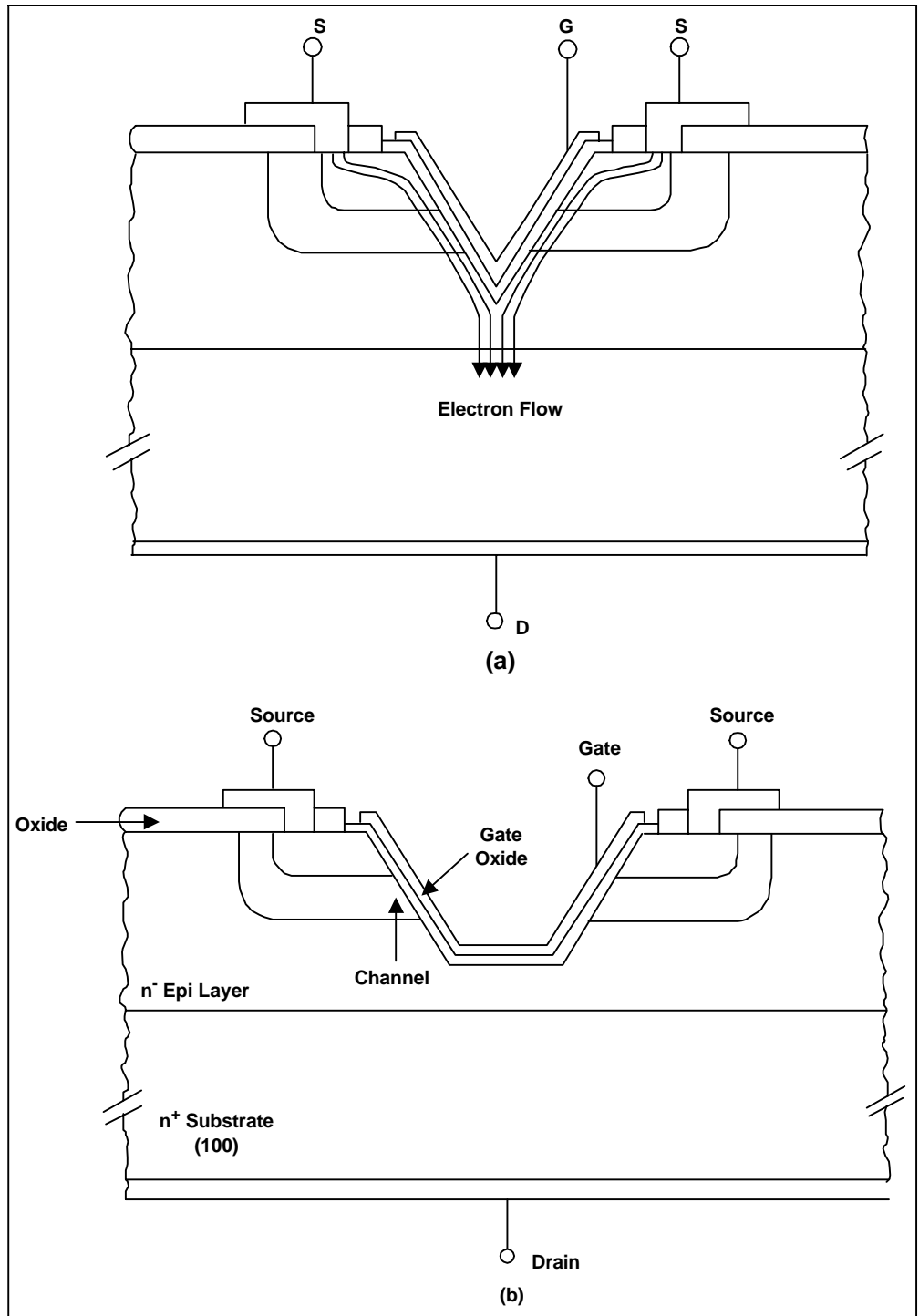


Figure 5. Trench MOSFET (a) Current Crowding in V-Groove Trench MOSFET, (b) Truncated V-Groove MOSFET

source and drain is denoted by I_{DSS} . There are tradeoffs to be made between $R_{DS(on)}$ that requires shorter channel lengths and punch-through avoidance that requires longer channel lengths.

The reach-through phenomenon occurs when the depletion region on the drift side of the body-drift p-n junction reaches the epilayer-substrate interface before avalanche takes place in the epi. Once the depletion edge enters the high carrier concentration substrate, a further increase in drain voltage will cause the electric field to quickly reach the critical value of 2×10^5 V/cm where avalanche begins.

ON-RESISTANCE

The on-state resistance of a power MOSFET is made up of several components as shown in Figure 8:

$$R_{DS(on)} = R_{source} + R_{ch} + R_A + R_J + R_D + R_{sub} + R_{wcml} \quad (1)$$

where:

R_{source} = Source diffusion resistance

R_{ch} = Channel resistance

R_A = Accumulation resistance

R_J = "JFET" component-resistance of the region between the two body regions

R_D = Drift region resistance

R_{sub} = Substrate resistance

Wafers with substrate resistivities of up to 20mΩ-cm are used for high voltage devices and less than 5mΩ-cm for low voltage devices.

R_{wcml} = Sum of Bond Wire resistance, the Contact resistance between the source and drain Metallization and the silicon, metallization and Leadframe contributions. These are normally negligible in high voltage devices but can become significant in low voltage devices.

Figure 9 shows the relative importance of each of the components to $R_{DS(on)}$ over the voltage spectrum. As can be seen, at high voltages the $R_{DS(on)}$ is dominated by epi resistance and JFET component. This component is higher in high voltage devices due to the higher resistivity or lower background carrier concentration in the epi. At lower voltages, the $R_{DS(on)}$ is dominated by the channel resistance and the contributions from the metal to semiconductor contact, metallization, bond wires and leadframe. The substrate contribution becomes more significant for lower breakdown voltage devices.

TRANSCONDUCTANCE

Transconductance, g_{fs} , is a measure of the sensitivity of drain current to changes in gate-source bias. This parameter is normally quoted for a V_{gs} that gives a drain current equal to about one half of the maximum current rating value and for a V_{DS} that ensures operation in the constant current region. Transconductance is influenced by gate width, which increases in proportion to the active area as cell density increases. Cell density has increased over the years from around half a million per square inch in 1980 to around eight million for planar MOSFETs and around 12 million for the trench technology. The limiting factor for even higher cell densities is the photolithography process control and resolution that allows contacts to be made to the source metallization in the center of the cells.

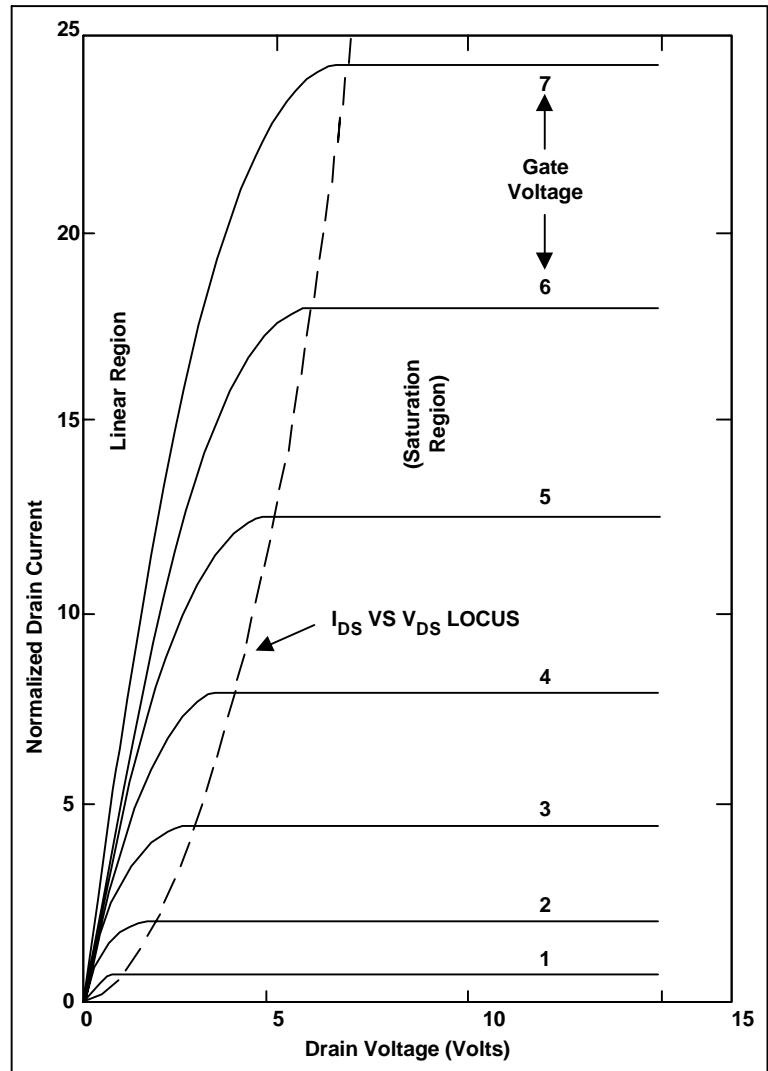


Figure 6. Current-Voltage Characteristics of Power MOSFET

Channel length also affects transconductance. Reduced channel length is beneficial to both g_{fs} and on-resistance, with punch-through as a tradeoff. The lower limit of this length is set by the ability to control the double-diffusion process and is around 1-2 μ m today. Finally the lower the gate oxide thickness the higher the g_{fs} .

THRESHOLD VOLTAGE

Threshold voltage, V_{th} , is defined as the minimum gate electrode bias required to strongly invert the surface under the poly and form a conducting channel between the source and the drain regions. V_{th} is usually measured at a drain-source current of 250 μ A. Common values are 2-4V for high voltage devices with thicker gate oxides, and 1-2V for lower voltage, logic-compatible devices with thinner gate oxides. With power MOSFETs finding increasing use in portable electronics and wireless communications where battery power is at a premium, the trend is toward lower values of $R_{DS(on)}$ and V_{th} .

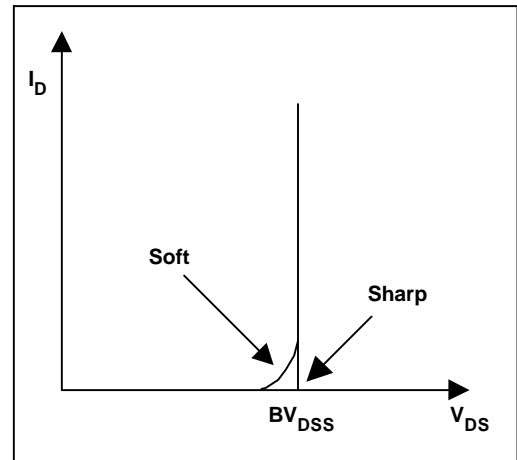


Figure 7. Power MOSFET Breakdown Characteristics

DIODE FORWARD VOLTAGE

The diode forward voltage, V_F , is the guaranteed maximum forward drop of the body-drain diode at a specified value of source current. Figure 10 shows a typical I-V characteristics for this diode at two temperatures. P-channel devices have a higher V_F due to the higher contact resistance between metal and p-silicon compared with n-type silicon. Maximum values of 1.6V for high voltage devices (>100V) and 1.0V for low voltage devices (<100V) are common.

POWER DISSIPATION

The maximum allowable power dissipation that will raise the die temperature to the maximum allowable when the case temperature is held at 25 $^{\circ}$ C is important. It is given by P_d where:

$$P_d = \frac{T_{jmax} - 25}{R_{thJC}} \quad (2)$$

T_{jmax} = Maximum allowable temperature of the p-n junction in the device (normally 150 $^{\circ}$ C or 175 $^{\circ}$ C)
 R_{thJC} = Junction-to-case thermal impedance of the device.

DYNAMIC CHARACTERISTICS

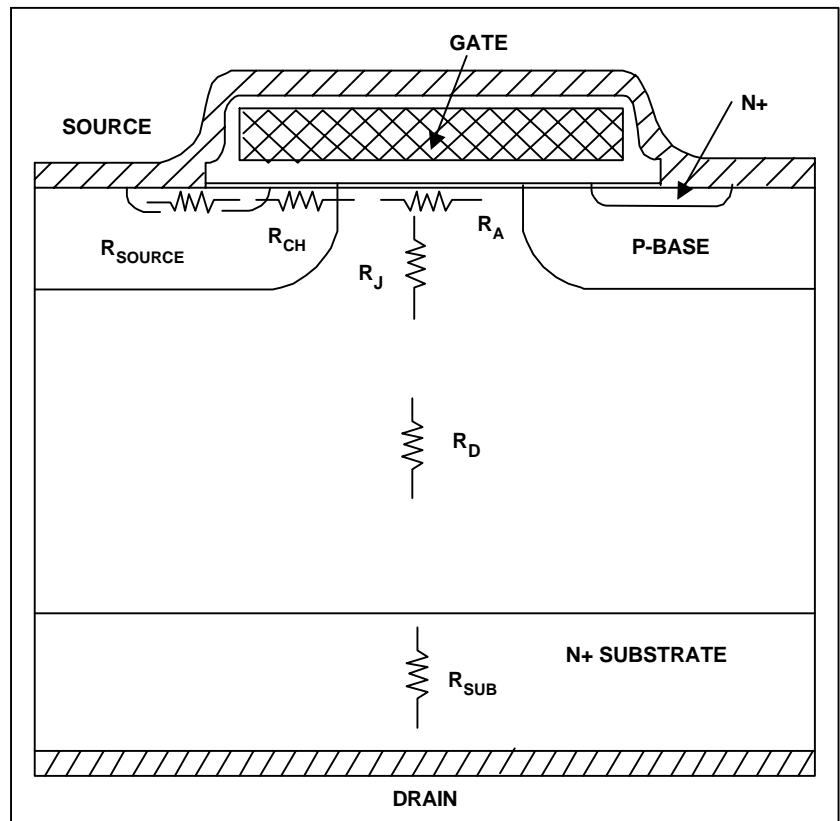


Figure 8. Origin of Internal Resistance in a Power MOSFET.

When the MOSFET is used as a switch, its basic function is to control the drain current by the gate voltage. Figure 11(a) shows the transfer characteristics and Figure 11(b) is an equivalent circuit model often used for the analysis of MOSFET switching performance.

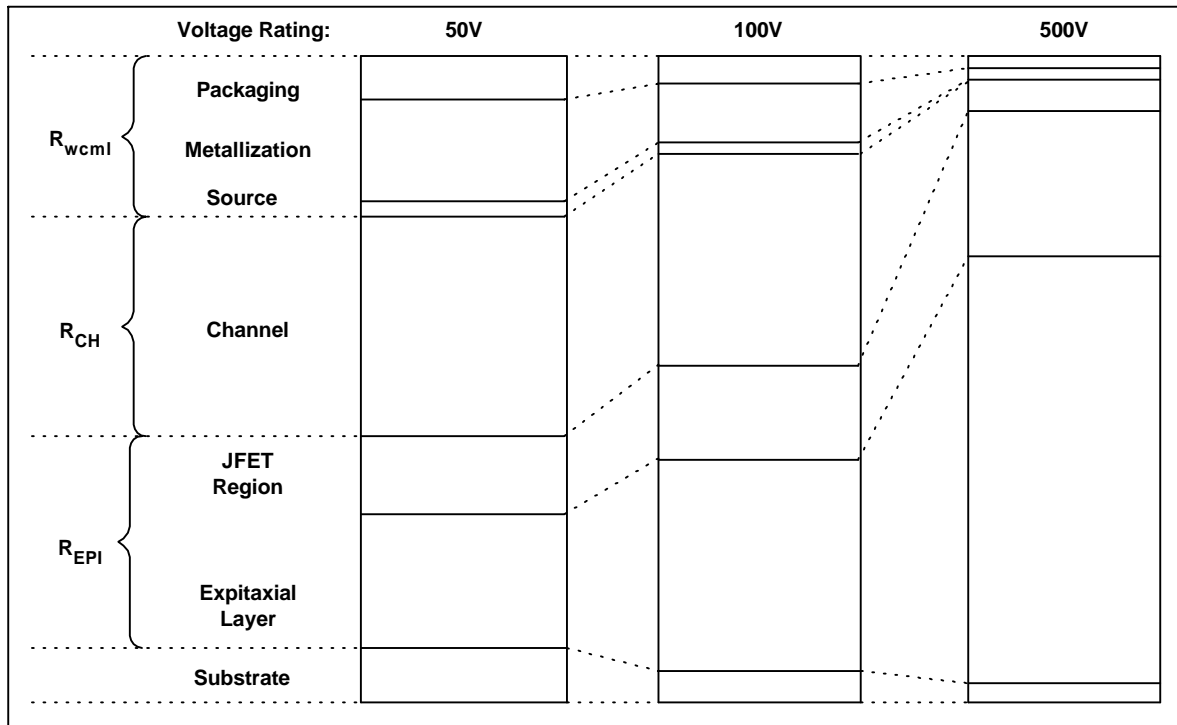


Figure 9. Relative Contributions to $R_{DS(on)}$ With Different Voltage Ratings.

The switching performance of a device is determined by the time required to establish voltage changes across capacitances. R_G is the distributed resistance of the gate and is approximately inversely proportional to active area. L_S and L_D are source and drain lead inductances and are around a few tens of nH. Typical values of input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances given in the data sheets are used by circuit designers as a starting point in determining circuit component values. The data sheet capacitances are defined in terms of the equivalent circuit capacitances as:

$$C_{iss} = C_{GS} + C_{GD}, C_{DS} \text{ shorted}$$

$$C_{rss} = C_{GD}$$

$$C_{oss} = C_{DS} + C_{GD}$$

Gate-to-drain capacitance, C_{GD} , is a nonlinear function of voltage and is the most important parameter because it provides a feedback loop between the output and the input of the circuit. C_{GD} is also called the Miller capacitance because it causes the total dynamic input capacitance to become greater than the sum of the static capacitances.

Figure 12 shows a typical switching time test circuit. Also shown are the components of the rise and fall times with reference to the V_{GS} and V_{DS} waveforms.

Turn-on delay, $t_{d(on)}$, is the time taken to charge the input capacitance of the device before drain current conduction can start. Similarly, turn-off delay, $t_{d(off)}$, is the time taken to discharge the capacitance after the after is switched off.

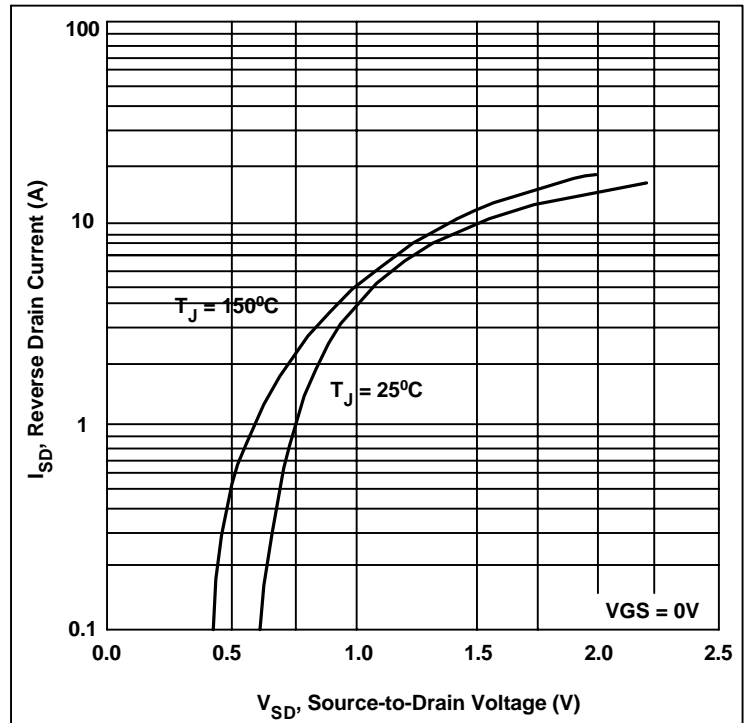


Figure 10. Typical Source-Drain (Body) Diode Forward Voltage Characteristics.

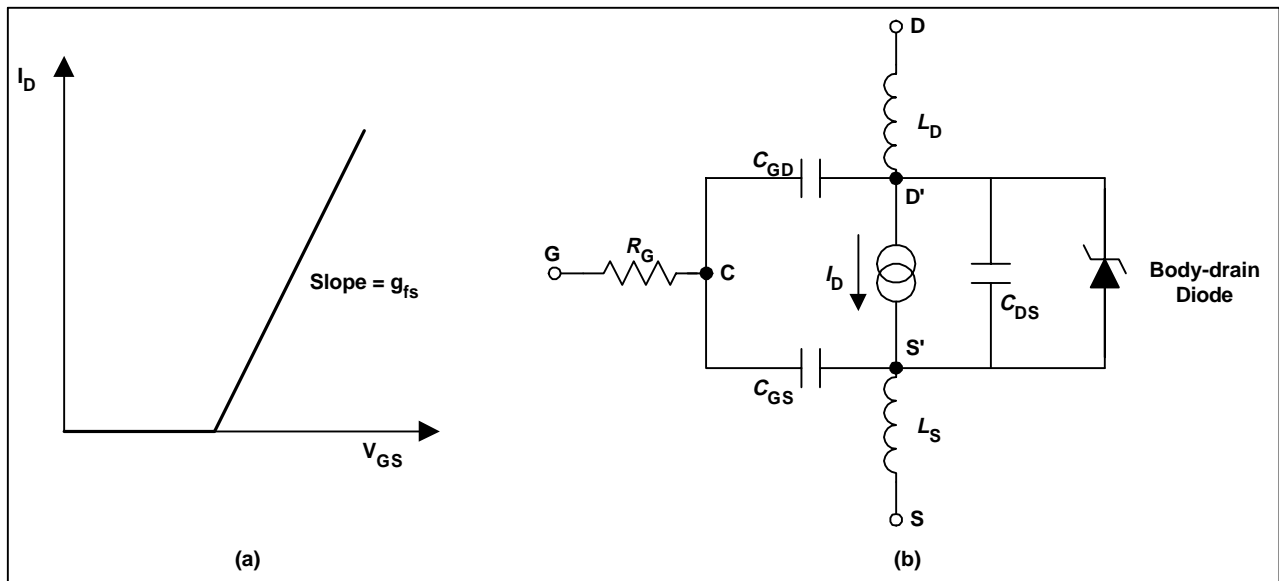


Figure 11. Power MOSFET (a) Transfer characteristics, (b) Equivalent Circuit Showing Components That Have Greatest Effect on Switching

GATE CHARGE

Although input capacitance values are useful, they do not provide accurate results when comparing the switching performances of two devices from different manufacturers. Effects of device size and transconductance make such comparisons more difficult. A more useful parameter from the circuit design point of view is the gate charge rather than capacitance. Most manufacturers include both parameters on their data sheets. Figure 13 shows a typical gate charge waveform and the test circuit. When the gate is connected to the supply voltage, V_{GS} starts to increase until it reaches V_{th} , at which point the drain current starts to flow and the C_{GS} starts to charge. During the period t_1 to t_2 , C_{GS} continues to charge, the gate voltage continues to rise and drain current rises proportionally. At time t_2 , C_{GS} is completely charged and the drain current reaches the predetermined current I_D and stays constant while the drain voltage starts to fall. With reference to the equivalent circuit model of the MOSFET shown in Figure 13, it can be seen that with C_{GS} fully charged at t_2 , V_{GS} becomes constant and the drive current starts to charge the Miller capacitance, C_{DG} . This continues until time t_3 .

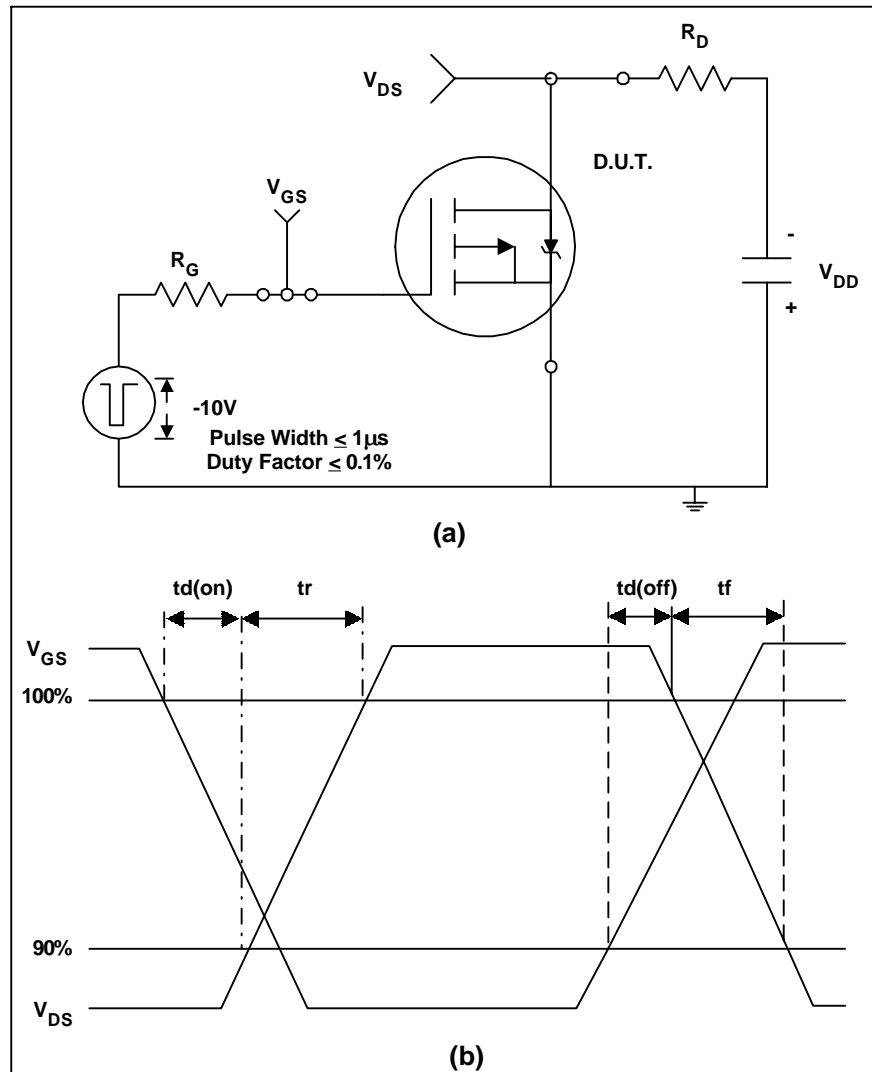


Figure 12. Switching Time Test (a) Circuit, (b) V_{GS} and V_{DS} Waveforms

Charge time for the Miller capacitance is larger than that for the gate to source capacitance C_{GS} due to the rapidly changing drain voltage between t_2 and t_3 (current = $C \, dv/dt$). Once both of the capacitances C_{GS} and C_{GD} are fully charged, gate voltage (V_{GS}) starts increasing again until it reaches the supply voltage at time t_4 . The gate charge ($Q_{GS} + Q_{GD}$) corresponding to time t_3 is the bare minimum charge required to switch the device on. Good circuit design practice dictates the use of a higher gate voltage than the bare minimum required for switching and therefore the gate charge used in the calculations is Q_G corresponding to t_4 .

The advantage of using gate charge is that the designer can easily calculate the amount of current required from the drive circuit to switch the device on in a desired length of time because $Q = CV$ and $I = C \, dv/dt$, the $Q = \text{Time} \times \text{current}$. For example, a device with a gate charge of 20nC can be turned on in $20\mu\text{sec}$ if 1mA is supplied to the gate or it can turn on in 20nsec if the gate current is increased to 1A . These simple calculations would not have been possible with input capacitance values.

dv/dt CAPABILITY

Peak diode recovery is defined as the maximum rate of rise of drain-source voltage allowed, i.e., dv/dt capability. If this rate is exceeded then the voltage across the gate-source terminals may become higher than the threshold voltage of the device, forcing the device into current conduction mode, and under certain conditions a catastrophic failure may occur. There are two possible mechanisms by which a dv/dt induced turn-on may take place. Figure 14 shows the equivalent circuit model of a power MOSFET, including the parasitic BJT. The first mechanism of dv/dt induced turn-on becomes active through the feedback action of the gate-drain capacitance, C_{GD} . When a voltage ramp appears across the drain and source terminal of the device a current I_1 flows through the gate resistance, R_G , by means of the gate-drain capacitance, C_{GD} . R_G is the total gate resistance in the circuit and the voltage drop across it is given by:

$$V_{GS} = I_1 R_G = R_G C_{GD} \frac{dv}{dt} \quad (3)$$

When the gate voltage V_{GS} exceeds the threshold voltage of the device V_{th} , the device is forced into conduction. The dv/dt capability for this mechanism is thus set by:

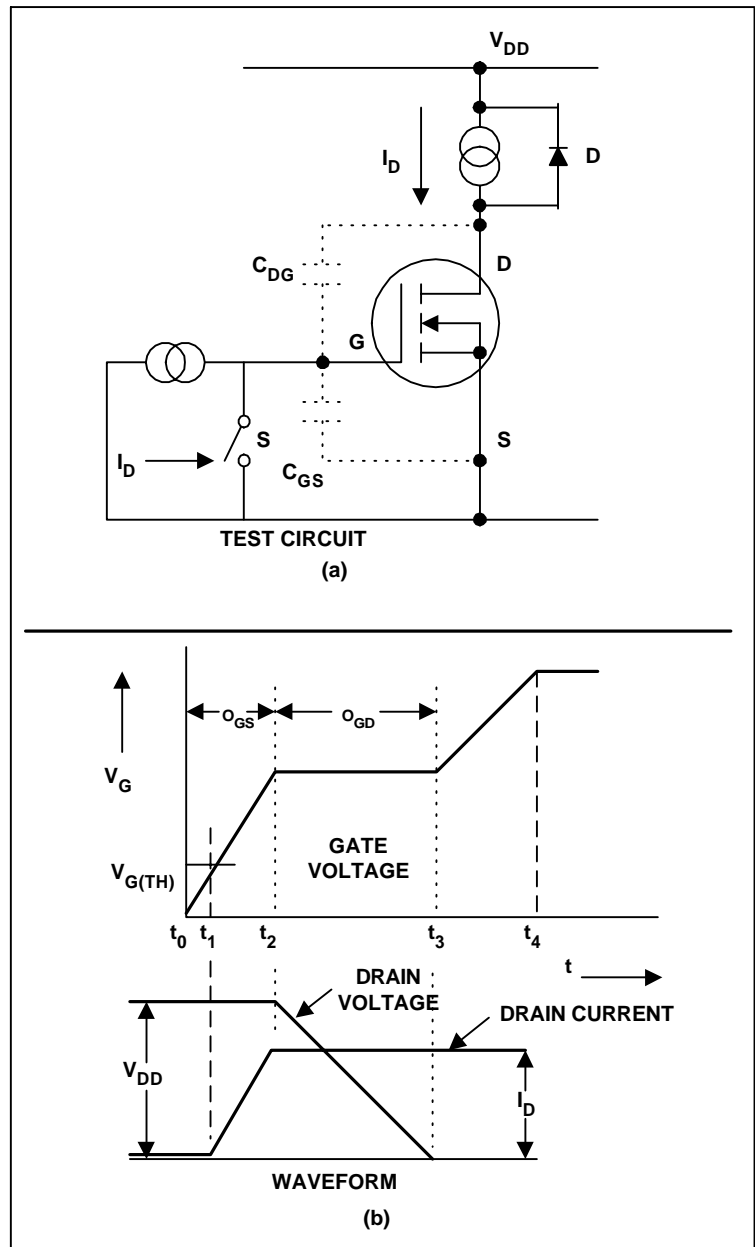


Figure 13. Gate Charge Test (a) Circuit, (b) Resulting Gate and Drain Waveforms.

$$\frac{dv}{dt} = \frac{V_{th}}{R_G C_{GD}} \quad (4)$$

It is clear that low V_{th} devices are more prone to dv/dt turn-on. The negative temperature coefficient of V_{th} is of special importance in applications where high temperature environments are present. Also gate circuit impedance has to be chosen carefully to avoid this effect.

The second mechanism for the dv/dt turn-on in MOSFETs is through the parasitic BJT as shown in Figure 15. The capacitance associated with the depletion region of the body diode extending into the drift region is denoted as C_{DB} and appears between

the base of the BJT and the drain of the MOSFET. This capacitance gives rise to a current I_2 to flow through the base resistance R_B when a voltage ramp appears across the drain-source terminals. With analogy to the first mechanism, the dv/dt capability of this mechanism is:

$$\frac{dv}{dt} = \frac{V_{BE}}{R_B C_{DB}} \quad (5)$$

If the voltage that develops across R_B is greater than about 0.7V, then the base-emitter junction is forward-biased and the parasitic BJT is turned on. Under the conditions of high (dv/dt) and large values of R_B , the breakdown voltage of the MOSFET will be limited to that of the open-base breakdown voltage of the BJT. If the applied drain voltage is greater than the open-base breakdown voltage, then the MOSFET will enter avalanche and may be destroyed if the current is not limited externally.

Increasing (dv/dt) capability therefore requires reducing the base resistance R_B by increasing the body region doping and reducing the distance current I_2 has to flow laterally before it is collected by the source metallization. As in the first mode, the BJT related dv/dt capability becomes worse at higher temperatures because R_B increases and V_{BE} decreases with increasing temperature.

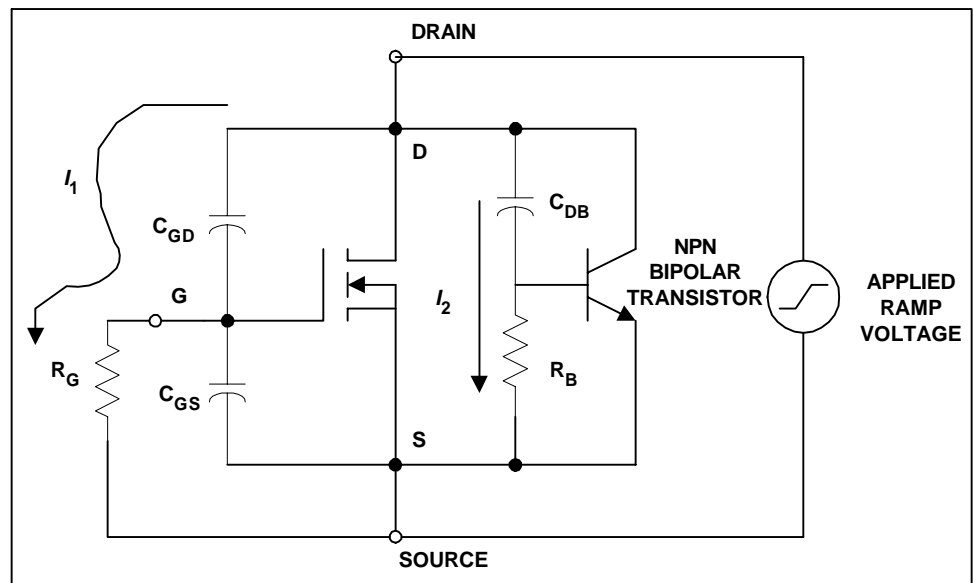


Figure 14. Equivalent Circuit of Power MOSFET Showing Two Possible Mechanisms for dv/dt Induced Turn-on.

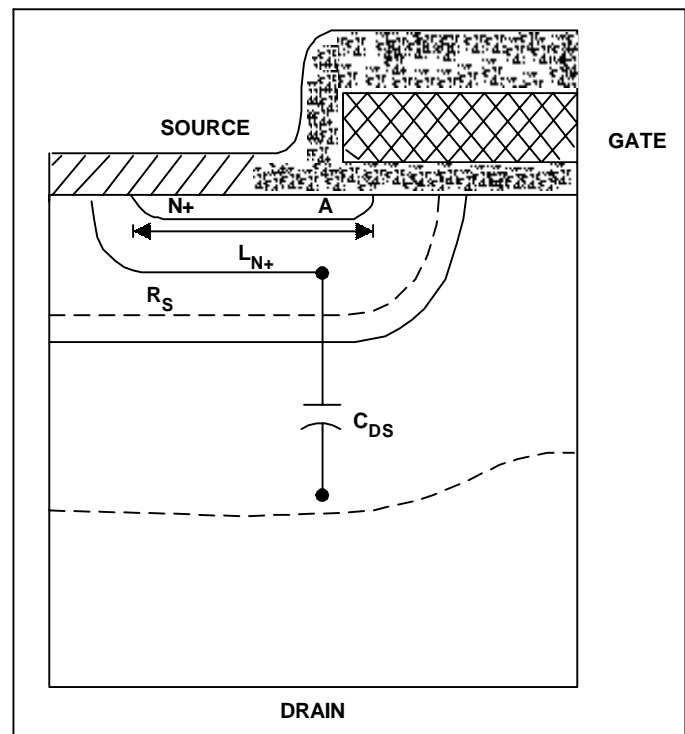


Figure 15. Physical Origin of the Parasitic BJT Components That May Cause dv/dt Induced Turn-on

References:

"HEXFET Power MOSFET Designer's Manual - Application Notes and Reliability Data," International Rectifier

"Modern Power Devices," B. Jayant Baliga

"Physics of Semiconductor Devices," S. M. Sze

"Power FETs and Their Applications," Edwin S. Oxner

"Power MOSFETs - Theory and Applications," Duncan A. Grant and John Gower



Introduction to Power MOSFETs and their Applications

INTRODUCTION

The Power MOSFETs that are available today perform the same function as Bipolar transistors except the former are voltage controlled in contrast to the current controlled Bipolar devices. Today MOSFETs owe their ever-increasing popularity to their high input impedance and to the fact that being a majority carrier device, they do not suffer from minority carrier storage time effects, thermal runaway, or second breakdown.

MOSFET OPERATION

An Understanding of the operation of MOSFETs can best be gleaned by the first considering the lateral N-channel MOSFET shown in Figure 1.

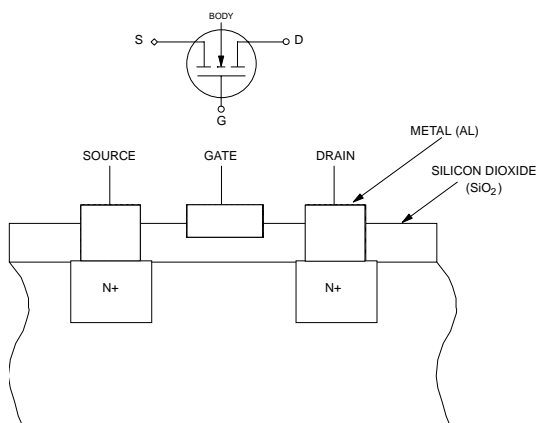


Figure 1. Lateral N-Channel MOSFET Cross-Section

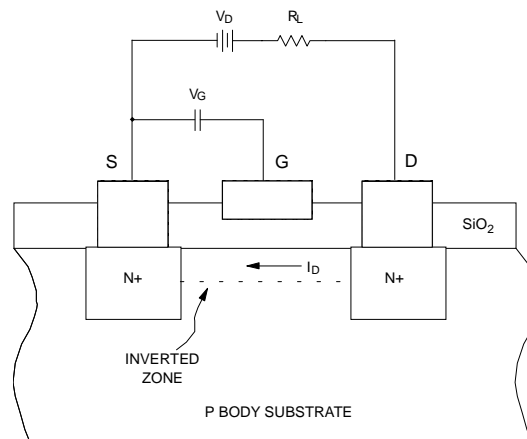


Figure 2. Lateral MOSFET Transistor Biased for Forward Current Conduction

With no electrical bias applied to the gate G, no current can flow in either direction underneath the gate because there will always be a blocking PN junction. When the gate is forward biased with respect to the source S together with an applied drain-source voltage, as shown in Figure 2, the free hole carriers in the p-epitaxial layer are repelled away from the gate area creating a channel, which allows electrons to flow from the source to the drain. Note that since the holes have been repelled from the gate channel, the electrons are the "majority carriers" by default. This mode of operation is called "enhancement" but is easier to think of enhancement mode of operation as the device being "normally off", i.e., the switch blocks the current until it receives a signal to turn on. The opposite is depletion mode, which is normally "on" device.

The advantages of the lateral MOSFET are:

1. Low gate signal power requirement. No gate current can flow into the gate after the small gate oxide capacitance has been charged.
2. Fast switching speeds because electrons can start to flow from drain to source as soon as the channel opens. The channel depth is proportional to the gate voltage and pinches closed as soon as the gate voltage is removed, so there is no storage time effect as occurs in transistors.

The major disadvantages are:

1. High resistance channels. In normal operation, the source is electrically connected to the substrate. With no gate bias, the depletion region extends out from the N+ drain in a pseudo-hemispherical shape. The channel length L cannot be made shorter than the minimum depletion width required to support the rated voltage of the device.
2. Channel resistance may be decreased by creating wider channels but this is costly since it uses up valuable silicon real estate. It also slows down the switching speed of the device by increasing its gate capacitance.

Enter vertical MOSFETs!

The Power MOSFET structure (also known as DMOS) is shown Figure 3.

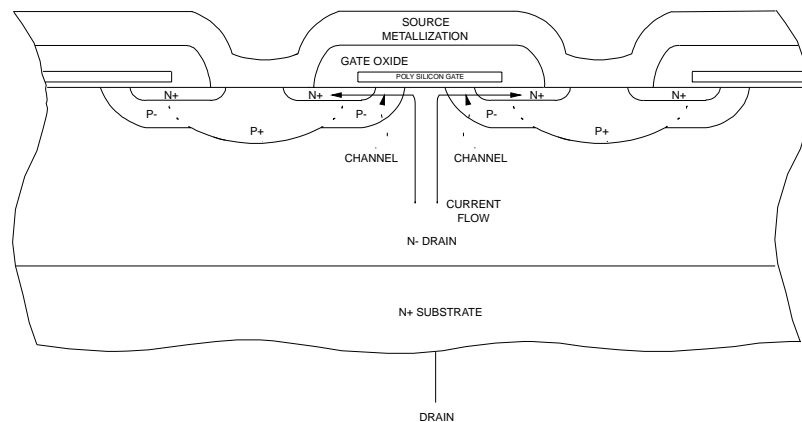


Figure 3. Vertical DMOS Cross-Sectional

The current path is created by inverting the p-layer underneath the gate by the identical method in the lateral MOSFETs. Source current flows underneath this gate area and then vertically through the drain, spreading out as it flows down. A typical MOSFET consists of many thousands of N+ sources conducting in parallel. This vertical geometry makes possible lower on-state resistances ($R_{DS(on)}$) for the same blocking voltage and faster switching than the lateral MOSFETs.

There are many vertical construction designs possible, e.g., V-groove and U-groove, and many source geometries, e.g. squares, triangles, hexagons, etc. The many considerations that determine the source geometry are $R_{DS(on)}$, input capacitance, switching times and transconductance.

PARASITIC DIODE

Early versions of MOSFETs were susceptible to voltage breakdown due to voltage transients and also had a tendency to turn on under high rates of rise of drain-to-source voltage (dV/dt). Both resulted in catastrophic failures. The dV/dt turn-on was due to the inherent parasitic NPN transistor incorporated within the MOSFET, shown schematically in Figure 4a. Current flow needed to charge up junction capacitance C_{DG} acts like base current to turn on the parasitic NPN.

The parasitic NPN action is suppressed by shorting the N+ source to the P+ body using the source metallization. This now creates an inherent PN diode anti-parallel to the MOSFET transistor (see Figure 4b). Because of its extensive junction area, the current ratings and thermal resistance of this diode exhibit a very long reverse recovery time and large reverse recovery current due to the long minority carrier lifetimes in the N-drain layer, which precludes the use of this

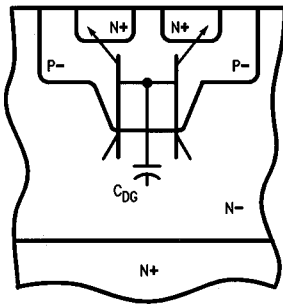


Figure 4a. DMOS Construction Showing Location of the Parasitic NPN Transistor

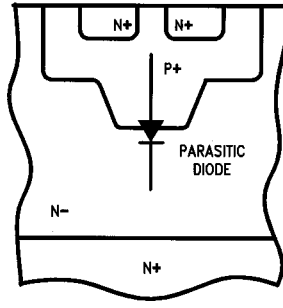


Figure 4b. Parasitic Diode

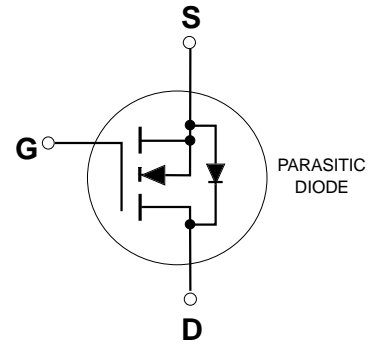


Figure 4c. Circuit Symbol

diodes except for very low frequency applications. e.g., motor control circuit shown in Figure 5. However in high frequency applications, the parasitic diode must be paralleled externally by an ultra-fast rectifier to ensure that the parasitic diode does not turn on. Allowing it to turn will substantially increase the device power dissipation due to the reverse recovery losses within the diode and also leads to higher voltage transients due to the larger reverse recovery current.

CONTROLLING THE MOSFET

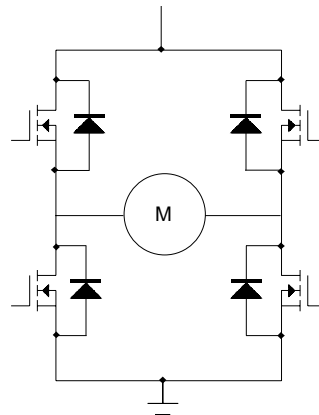


Figure 5. Full-Wave Motor Control Circuit

A major advantage of the Power MOSFET is its very fast switching speeds. The drain current is strictly proportional to gate voltage so that the theoretically perfect device could switch in 50ps - 200ps, the time it takes the carriers to flow from source to drain. Since the MOSFET is a majority carrier device, a second reason why it can outperform the junction transistor is that its turn-off is not delayed by minority carrier storage time in the base. A MOSFET begins to turn off as soon as its gate voltage drops down to its threshold voltage.

SWITCHING BEHAVIOR

Figure 6 illustrates a simplified model for the parasitic capacitances of a Power MOSFET and switching voltage waveforms with a resistive load. There are several different phenomena occurring during turn-on. Referring to the same figure:

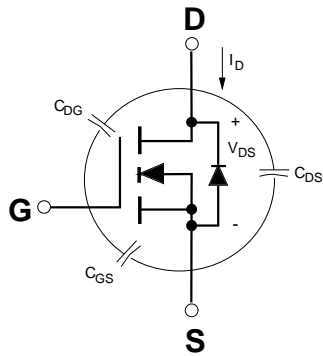


Figure 6a. MOSFET Capacitance Model for Power MOSFET

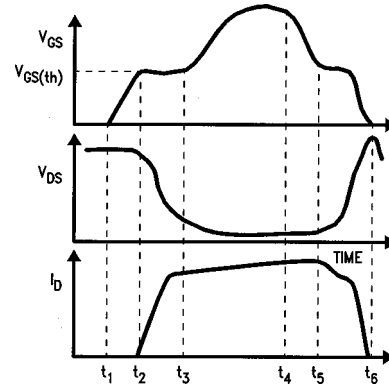


Figure 6b. Switching Waveforms for Resistive Load

Time interval $t_1 < t < t_2$:

The initial turn-on delay time $t_{d(ON)}$ is due to the length of time it takes V_{GS} to rise exponentially to the threshold voltage $V_{GS(TH)}$. From Figure 6, the time constant can be seen to be $R_S \times C_{GS}$.

Typical turn-on delay approximation is:

$$t_{d(on)} = R_S \times C_S \times 1n \left(1 - \frac{V_{GSIM}}{V_{PK}} \right) \quad (1)$$

Note that since the signal source impedance appears in the t_d equation, it is very important to pay attention to the test conditions used in measuring switching times.

Physically one can only measure input capacitance C_{iSS} , which consists of C_{GS} in parallel with C_{DG} . Even though $C_{GS} \gg C_{DG}$, the later capacitance undergoes a much larger voltage excursion so its effect on switching time cannot be neglected.

Plots of C_{iSS} , C_{OSS} , and C_{RSS} for the Fairchild Semiconductor Supersot™ NDS351N are shown in Figure 7 below. The charging and discharging of C_{DG} is analogous to the “Miller” effect that was first discovered with electron tubes and dominates the next switching interval.

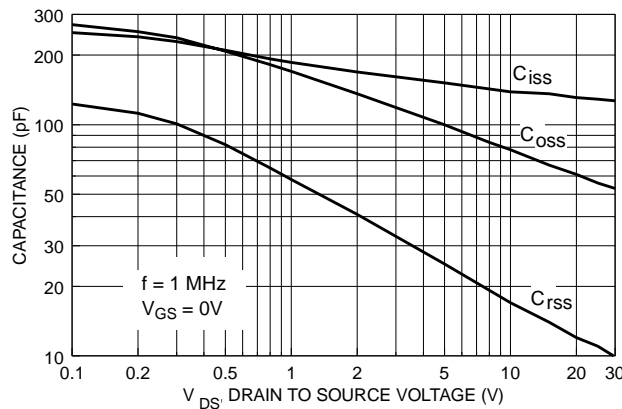


Figure 7. Typical Capacitances of NDS351N

Time interval $t_2 < t < t_3$:

Since V_{GS} has now achieved the threshold value, the MOSFET begins to draw increasing load current and V_{DS} decreases. C_{DG} must not only discharge but its capacitance value also increases since it is inversely proportional to V_{DS} , namely:

$$C_{DG} = \frac{C_{DG}(0)}{V_{DS}^n} \quad (2)$$

Unless the gate driver can quickly supply the current required to discharge C_{DG} , voltage fall will be slowed with increases in turn-on time.

Time interval $t_3 < t < t_4$:

The MOSFET is now on so the gate voltage can rise to the overdrive level.

Turn-off interval $t_4 < t < t_6$:

Turn-off occurs in reverse order. V_{GS} must drop back close to the threshold value before $R_{DS(on)}$ will start to increase. As V_{DS} starts to rise, the Miller effect due to C_{DG} re-occurs and impedes the rise of V_{DS} as C_{DG} recharges to V_{CC} .

Specific gate drive circuits for different applications are discussed and illustrated later in this paper.

MOSFET CHARACTERIZATION

The output characteristics (I_D vs V_{DS}) of the Fairchild Semiconductor Supersot™ NDS351N are illustrated in Figures 8 and 9. The two distinct regions of operation in Figure 8 have been labeled “linear” and “saturated”. To understand the difference, recall that the actual current path in a MOSFET is horizontal through the channel created under the gate oxide and then vertical through the drain. In the linear region of operation, the voltage across the MOSFET channel is not sufficient for the carriers to reach their maximum current density. The static $R_{DS(on)}$, defined simply as V_{DS}/I_{DS} , is a constant.

As V_{DS} is increased, the carriers reach their maximum drift velocity and the current amplitude cannot increase. Since the device is behaving like a current generator, it is said to have high output impedance. This is the so-called “saturation” regions. One should also note that in comparing MOSFET operation to Bipolar transistor, the linear and saturated regions are just the opposite to the MOSFET. The equal spacing between the output I_D curves for constant step in V_{GS} indicates that the transfer characteristics in Figure 9 will be linear in the saturated region.

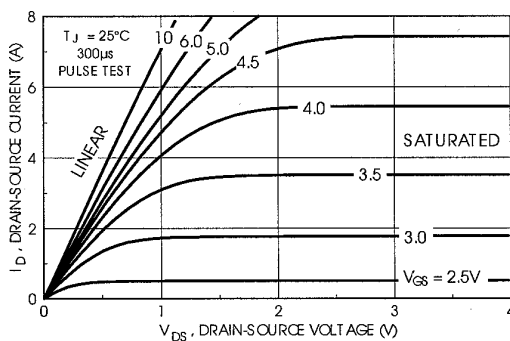


Figure 8. NDS351N Output Characteristics

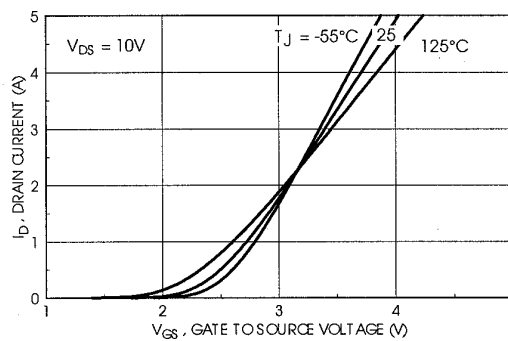


Figure 9. NDS351N Transfer Characteristics

IMPORTANCE OF THRESHOLD VOLTAGE

Threshold voltage $V_{GS(th)}$ is the minimum gate voltage that initiates drain current flow. $V_{GS(th)}$ can be easily measured on a Tektronix 576 curve tracer by connecting the gate to the drain and recording the required drain voltage for a specified drain current, typically $250\mu A$. $V_{GS(th)}$ in Figure 9 is 1.6V. While a high value of $V_{GS(th)}$, can apparently lengthen turn-on delay time, a low value for Power MOSFET is undesirable for the following reasons:

1. $V_{GS(th)}$ decreases with increased temperature.
2. The high gate impedance of a MOSFET makes it susceptible to spurious turn-on due to gate noise.
3. One of the more common modes of failure is gate-oxide voltage punch-through. Low $V_{GS(th)}$ requires thinner oxides, which lowers the gate oxide voltage rating.

POWER MOSFET THERMAL MODEL

Like all other power semiconductor devices, MOSFETs operate at elevated junction temperature. It is important to observe their thermal limitations in order to achieve acceptable performance and reliability. Specification sheets contain information on maximum junction temperature ($T_{J(max)}$), safe operating areas, current ratings and electrical characteristics as a function of T_J where appropriate. However, since it is still not possible to cover all contingencies, it is still important that the designer perform some junction calculations to ensure that the device operates within specifications.

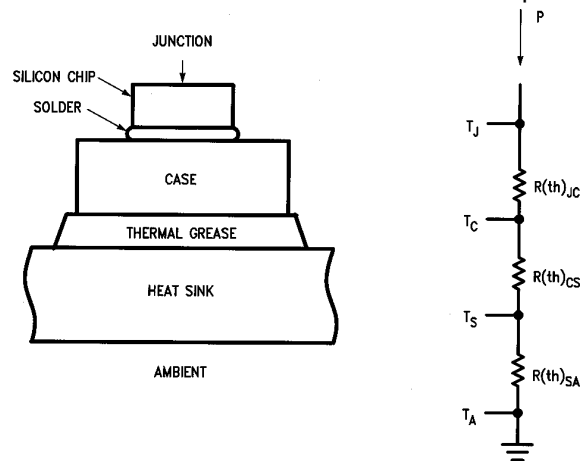


Figure10. MOSFET Steady-State Thermal Resistance Model

Figure 10 shows an elementary, steady-state, thermal model for any power semiconductor and the electrical analogue. The heat generated at the junction flows through the silicon pellet to the case or tab and then to the heat sink. The junction temperature rise above the surrounding environment is directly proportional to this heat flow and the junction-to-ambient thermal resistance. The following equation defined the steady-state thermal resistance $R_{\theta JA}$ between device junction to ambient:

$$R_{\theta JA} = \frac{T_J - T_A}{P} \quad (3)$$

where:

T_J = average temperature at the device junction ($^{\circ}C$)

T_A = average temperature at ambient ($^{\circ}C$)

P = average heat flow in watts (W).

Note that for thermal resistance to be meaningful, two temperature reference points must be specified. Units for $R_{\theta JA}$ are $^{\circ}C/W$.

The thermal model shows symbolically the locations for the reference points of junction temperature, case temperature, sink temperature and ambient temperature. These temperature reference define the following thermal resistances:

$R_{\theta JC}$: Junction-to-Case thermal resistance.

$R_{\theta CS}$: Case-to-Sink thermal resistance.

$R_{\theta SA}$: Sink-to-Ambient thermal resistance.

Since the thermal resistances are in series:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (4)$$

The design and manufacture of the device determines $R_{\theta JC}$ so that while $R_{\theta JC}$ will vary somewhat from device to device, it is the SOLE RESPONSIBILITY of the manufacturer to guarantee a maximum value for $R_{\theta JC}$. Both the user and manufacturer must cooperate in keeping $R_{\theta CS}$ to an acceptable maximum. Finally, the user has sole responsibility for the external heat sinking.

By inspection of Figure 10, one can write an expression for T_J :

$$T_J = T_A + P \times (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) \quad (5)$$

While this appears to be a very simple formula, the major problem using it is due to the fact that the power dissipated by the MOSFET depends upon T_J . Consequently one must use either an iterative or graphical solution to find the maximum $R_{\theta SA}$ to ensure stability. But an explanation of transient thermal resistance is in order to handle the case of pulsed applications.

Use of steady-state thermal resistance is not satisfactory for finding peak junction temperatures for pulsed applications. Plugging in the peak power value results in overestimating the actual junction temperature while using the average power value underestimates the peak junction temperature at the end of the power pulse. The reason for the discrepancy lies in the thermal capacity of the semiconductor and its housing, i.e., its ability to store heat and to cool down before the next pulse.

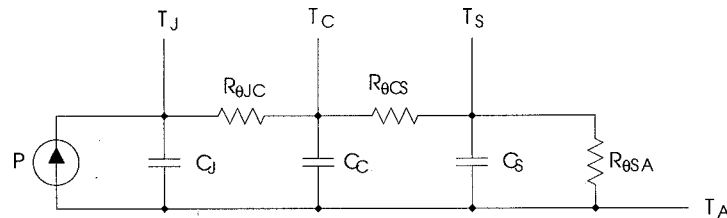


Figure 11. Transient Thermal Resistance Model

The modified thermal model for the MOSFET is shown in Figure 11. The normally distributed thermal capacitances have been lumped into single capacitors labeled C_J , C_C , and C_S . This simplification assumes current is evenly distributed across the silicon chip and that the only significant power losses occur in the junction. When a step pulse of heating power, P , is introduced at the junction, figure 12a shows that T_J will rise at an exponential rate to some steady state value dependent upon the response of the thermal network. When the power input is terminated at time t_2 , T_J will decrease along the curve indicated by T_{cool} in Figure 12a back to its initial value. Transient thermal resistance at time t is thus defined as:

$$Z_{\theta JC} = \frac{\Delta T_{JC}(t)}{P} \quad (6)$$

The transient thermal resistance curve approaches the steady-state value at long times and the slope of the curve for short times is inversely proportional to C_J . In order to use this curve

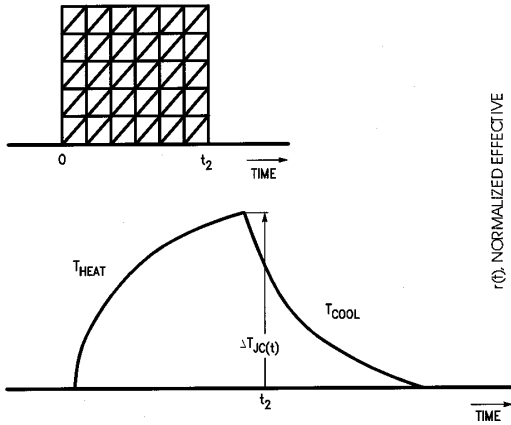


Figure 12a. Junction Temperature Response to a Step Pulse of Heating Power

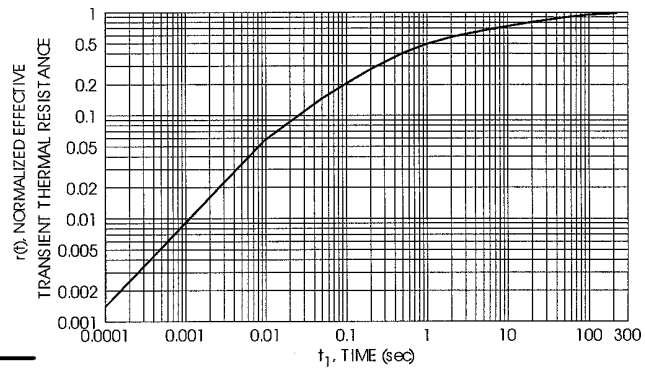


Figure 12b. Transient Thermal Resistance Curve for NDS351N

with confidence, it must represent the highest values $Z_{\theta JC}$ for each time interval that can be expected from the manufacturing distribution of the products.

While predicting T_J in response to a series of power pulses becomes very complex, superposition of power pulses offers a rigorous numerical method of using the transient thermal resistance curve to secure a solution. Superposition tests the response of a network to any input function by replacing the input with an equivalent series of superimposed positive and negative step functions. Each step function must start from zero and continue to the time for which T_J is to be computed. For example, Figure 13 illustrates a typical train of heating pulses.

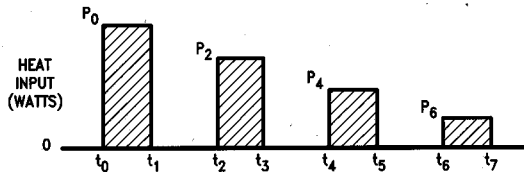


Figure 13a. Heat Input

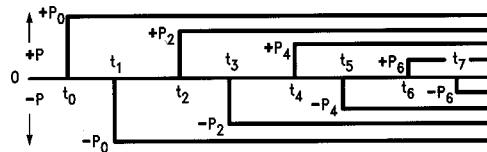


Figure 13b. Equivalent Heat Input by Superposition of Power Pulses

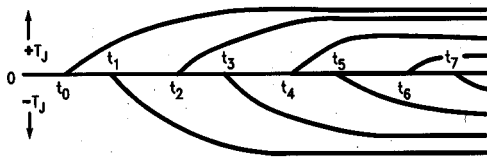


Figure 13c. Junction Temperature Response to Individual Power Pulse

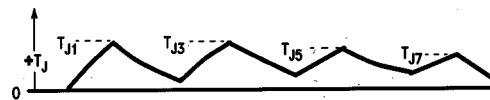


Figure 13d. Use of Superposition to Determine Peak T_J

T_J at time is given by:

$$T_J(t) = T_J(0) + \sum P_i \times [Z_{\theta JC}(t_n - t_i) - Z_{\theta JC}(t_n - t_i + 1)] \quad (7)$$

The typical use condition is to compute the peak junction temperature at thermal equilibrium for a train of equal amplitude power pulses as shown in Figure 14.

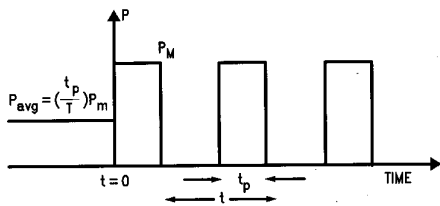


Figure 14a. Train of Power Pulses

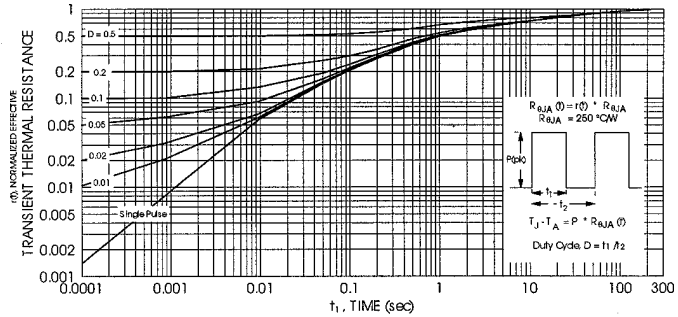


Figure 14b. Normalized $r(t)$ for NDS351N

To further simplify this calculation, the bracketed expression in equation (G) has been plotted for all Fairchild Semiconductor Power MOSFETs, as exemplified by the plot of $Z_{\theta JC}$ in Figure 14b. From this curve, one can readily calculate T_J if one knows P_M , $Z_{\theta JC}$ and T_C using the expression:

$$T_J = T_C + P_M \times Z_{\theta JC} \quad (8)$$

Example: Compute the maximum junction temperature for a train of 1W, 10ms wide heating pulses repeated every 100ms. Assume a case temperature of 55°C.

Duty factor=0.1

From Figure 14b: $Z_{\theta JC} = 0.14 \times 250^\circ\text{C/W} = 35^\circ\text{C/W}$

Substituting into Equation (7):

$$T_{J(\max)} = 55 + 1 \times 35 = 90^\circ\text{C}$$

SAFE OPERATING AREA

The Power MOSFET is not subjected to forward or reverse bias second breakdown, which can easily occur in transistors. Second breakdown is a potentially catastrophic condition in transistors caused by thermal hot spots in the silicon as the transistor turns on or off. However in the MOSFET, the carriers travel through the device much as if it were a bulk semiconductor, which exhibits positive temperature coefficient. If current attempts to self-constrict to a localized area, the increasing temperature of the spot will raise the spot resistance due to positive temperature coefficient of the bulk silicon. The ensuing higher voltage drop will tend to redistribute the current away from the hot spot. Figure 15 shows the safe operating area of the Fairchild Semiconductor Supersot™ NDS351N device.

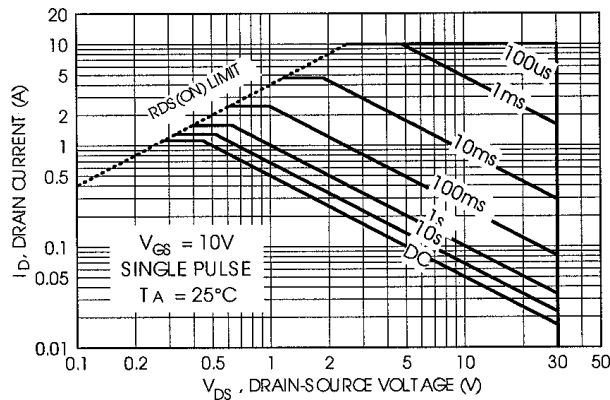


Figure 15. Safe Operating Area of NDS351N

Note that the safe area boundaries are only thermally limited and exhibit no derating for second breakdown. This shows that while the MOSFET transistor is very rugged, it may still be destroyed thermally by forcing it to dissipate too much power.

ON-RESISTANCE $R_{DS(on)}$

The on-resistance of a Power MOSFET is a very important parameter because it determines how much current the device can carry for low to medium frequency (less than 200kHz) applications. After being turned on, the on-state is defined simply as its on-state voltage divided by on-state current. When conducting current as a switch, the conduction losses P are:

$$P_C = I_{D(RMS)}^2 \times R_{DS(on)} \quad (9)$$

To minimize $R_{DS(on)}$, the applied gate signal should be large enough to maintain operation in the linear or ohmic region as shown in Figure 8. Fairchild Semiconductor SUPERSOT™-3 NDS351N will conduct its rated current for $V_{GS}=4.5V$, which is also the value used to generate the curves of $R_{DS(on)}$ vs I_D and T_J that are shown in Figure 16 for the Fairchild Semiconductor Supersot NDS351N. Since $R_{DS(on)}$ is a function of T_J , Figure 16 plots this parameter at various junction temperatures. Note that as the drain current rises, $R_{DS(on)}$ increases once I_D exceeds the rated current value. Because the MOSFET is a majority carrier device, the component of $R_{DS(on)}$ due to the bulk resistance of the N- silicon in the drain region increases with temperature as well. While this must be taken into account to avoid thermal runaway, it does facilitate parallel operation of MOSFETs. Any imbalance between MOSFETs does not result in current hogging because the device with the most current heat up and ensuing higher on-voltage will divert some current to the other devices in parallel.

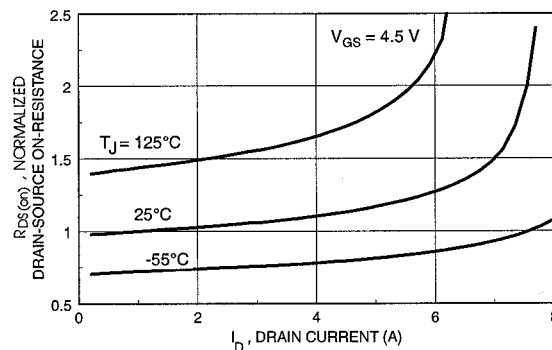


Figure 16. $R_{DS(on)}$ of NDS351N

TRANSCONDUCTANCE

Since MOSFETs are voltage controlled, it has become necessary to resurrect the term transconductance g_{FS} , commonly used in the past with electron tubes. Referring to Figure 8, g_{FS} equals to the change in drain current divided by the change in gate voltage for a constant drain voltage. Mathematically:

$$g_{fs}(\text{Siemens}) = \frac{dI_D(A)}{dV_{GS}(V)} \quad (10)$$

Transconductance varies with operating conditions, starting at 0 for $V_{GS} < V_{GS(th)}$ and peaking at a finite value when the device is fully saturated. It is very small in the ohmic region because the device cannot conduct any more current. Transconductance is useful in designing linear amplifiers and does not have any significance in switching power supplies.

GATE DRIVE CIRCUITS FOR POWER MOSFETS

The drive circuit for a Power MOSFET will affect its switching behavior and its power dissipation. Consequently the type of drive circuitry depends upon the application. If on-state power losses due to $R_{DS(on)}$, will predominate, there is little point in designing a costly drive circuit. This power dissipation is relatively independent of gate drive as long as the gate-source voltage exceeds the threshold voltage by several volts and an elaborate drive circuit to decrease switching times will only create additional EMI and voltage ringing. In contrast, the drive circuit for a device switching at 200KHz or more will affect the power dissipation since switching losses are a significant part of the total power dissipation.

Compare to a junction transistor, the switching losses in a MOSFET can be made much smaller but these losses must still be taken into consideration. Examples of several typical loads along with the idealized switching waveforms and expressions for power dissipation are given in Figure 17 to 19.

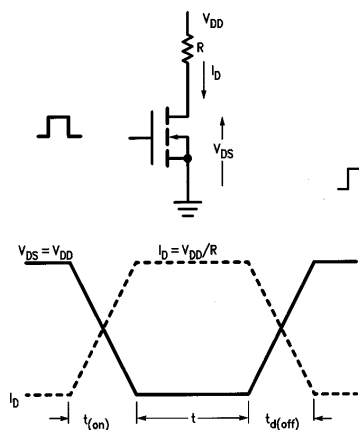


Figure 17. Resistive Load Switching Waveforms

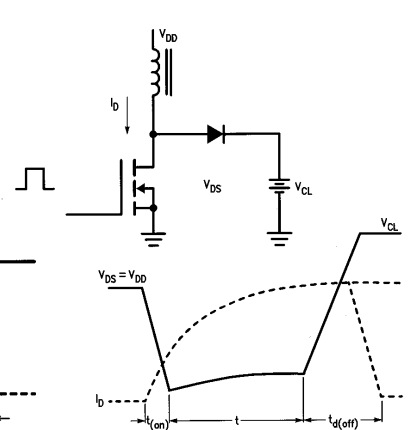


Figure 18. Clamped Inductive Load Switching Waveforms

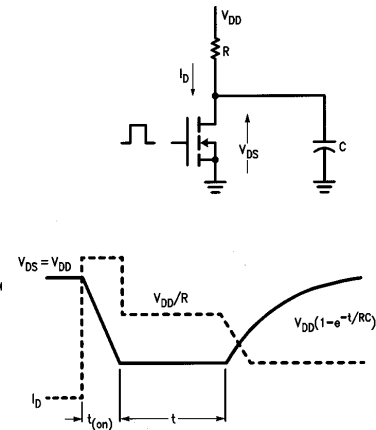


Figure 19. Capacitive Load Switching Waveforms

Their power losses can be calculated from the general expression:

$$P_D = \left(\frac{1}{T}\right) \int I_D(t) \times V_{DS}(t) dt \times f_s \quad (11)$$

where f_s = Switching frequency.

For the idealized waveforms shown in the figures, the integration can be approximated by the calculating areas of triangles:

Resistive loads:

$$P_D = \frac{V_{DD}^2}{R} \left[\frac{t_{on} + t_{off}}{6} + R_{DS(on)} \times T \right] \times f_s$$

Inductive Load:

$$P_D = \frac{V_{CL} \times I_m \times t_{off} \times f_s}{2} + P_C \quad \text{where } P_C = \text{conduction loss during period } T.$$

Capacitive load:

$$P_D = \left(\frac{C \times V_{DD}}{2} + \frac{V_{DD}^2 \times R_{DS(on)}}{R^2} \times T \right) \times f_S$$

Gate losses and blocking losses can usually be neglected. Using these equations, circuit designer is able to estimate the required heat sink. A final heat run in a controlled temperature environment is necessary to ensure thermal stability.

Since a MOSFET is essentially voltage controlled, the only gate current required is that necessary to charge the input capacitance C_{iss} . In contrast to a 10A transistor, which may require a base current of 2A to ensure saturation, a Power MOSFET can be driven directly by CMOS or open-collector TTL logic circuit similar to that in Figure 20.

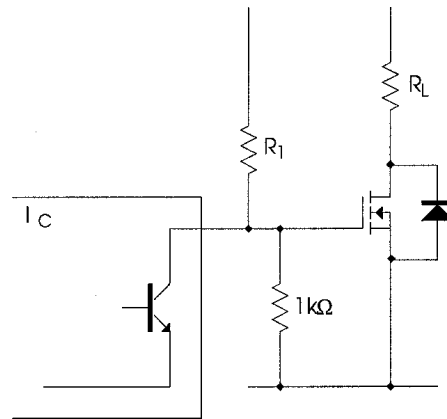


Figure 20. Open Collector TTL Drive Circuit

Turn-on speed depends upon the selection of resistor R_1 , whose minimum value will be determined by the current sinking rating of the IC. It is essential that an open collector TTL buffer be used since the voltage applied to the gate must exceed the MOSFET threshold voltage. CMOS devices can be used to drive the power device directly since they are capable of operating 15V supplies.

Interface ICs, originally intended for other applications, can be used to drive the Power MOSFETs, as shown below in Figure 21.

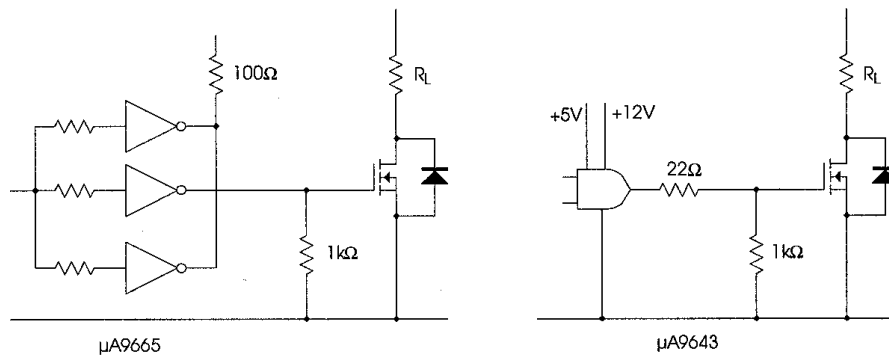


Figure 21. Interface ICs Used to Drive Power MOSFETs

Most frequently, switching power supply applications employ a pulse width modulator IC with an NPN transistor output stage. This output transistor is ON when the MOSFET should be ON, hence the type of drive used with open-collector TTL devices cannot be used. Figures 22 and 23 give examples of typical drive circuits used with PWM ICs.

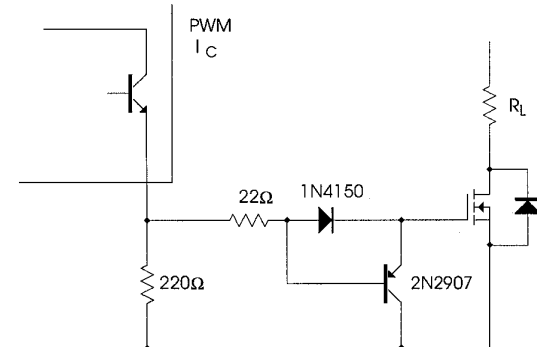


Figure 22. Circuit for PWM IC Driving MOSFET. The PNP Transistor Speeds Up Turn-Off

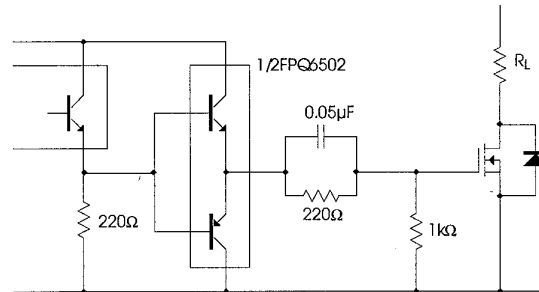


Figure 23. Emitter Follower with Speed-Up Capacitor

Isolation: Off-line switching power supplies use power MOSFETs in a half bridge configuration because inexpensive, high voltage devices with low $R_{DS(on)}$ are not available.

Since one of the power devices is connected to the positive rail, its drive circuitry is also floating at a high potential. The most versatile method of coupling the drive circuitry is to use a pulse transformer. Pulse transformers are also normally used to isolate the logic circuitry from the MOSFETs operating at high voltage to protect it from a MOSFET failure.

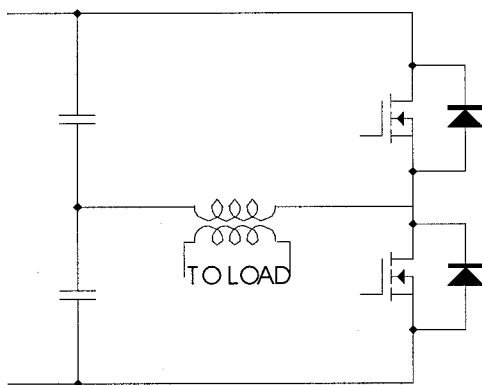


Figure 24. Half-Bridge Configuration

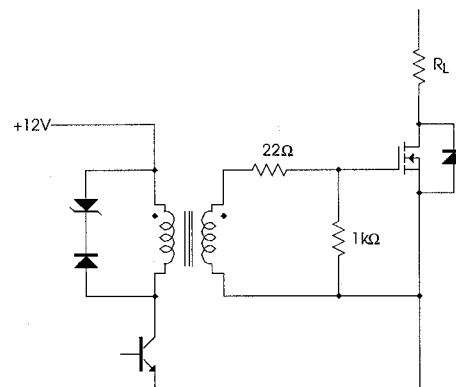


Figure 25. Simple Pulse Transformer Drive Circuit. The Transistor May Be a Part of a PWM IC if Applicable

The zener diodes shown in Figure 25 is included to reset the pulse transformer quickly. The duty cycle can approach 50% with a 12V zener diode. For better performance at turn-off, a PNP transistor can be added as shown in Figure 26.

Figure 27 illustrates an alternate method to reverse bias the MOSFET during turn-off by inserting a capacitor in series with the pulse transformer. The capacitor also ensures that the pulse transformer will not saturate due to DC bias.

Opto-isolators may also be used to drive power MOSFETs but their long switching times make them suitable only for low frequency applications.

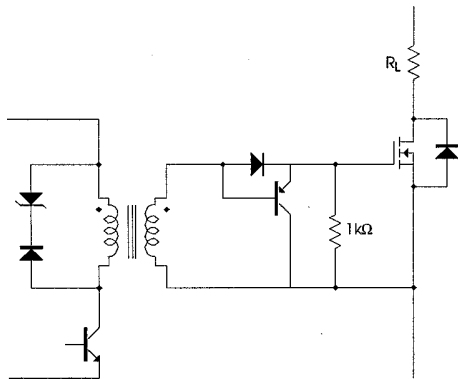


Figure 26. Improved Performance at Turn-Off with a Transistor

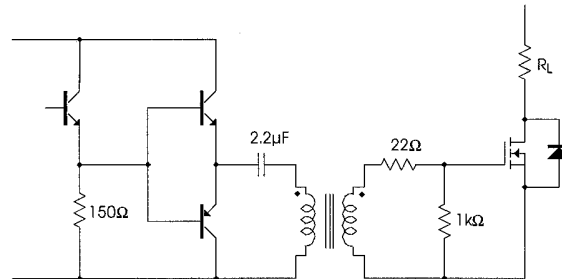


Figure 27. Emitter Follower Driver with Speed-Up Capacitor

SELECTING A DRIVE CIRCUIT

Any of the circuits shown are capable of turning a Power MOSFET on and off. The type of circuit depends upon the application. The current sinking and sourcing capabilities of the drive circuit will determine the switching time and switching losses of the power device. As a rule, the higher the gate current at turn-on and turn-off, the lower the switching losses will be. However, fast drive circuits may produce ringing in the gate circuit and drain circuits. At turn-on, ringing in the gate circuit may produce a voltage transient in excess of the maximum V_{GS} rating, which will puncture the gate oxide and destroy it. To prevent this occurrence, a zener diode of appropriate value may be added to the circuit as shown in Figure 28. Note that the zener should be mounted as close as possible to the device.

At turn-off, the gate voltage may ring back up to the threshold voltage and turn on the device for a short period. There is also the possibility that the drain-source voltage will exceed its maximum rated voltage due to ringing in the drain circuit. A protective RC snubber circuit or zener diode may be added to limit drain voltage to a safe level.

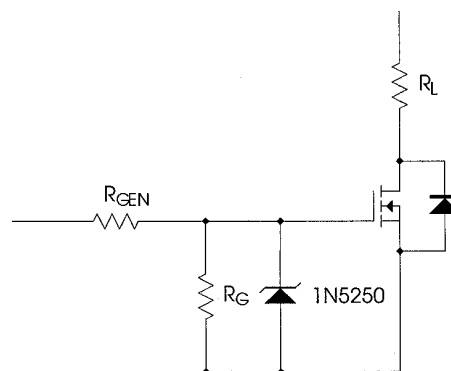


Figure 28. Zener Diode to Prevent Excessive Gate-Source Voltages

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	ISOPLANAR™
CoolFET™	MICROWIRE™
CROSSVOLT™	POP™
E ² CMOS™	PowerTrench™
FACT™	QS™
FACT Quiet Series™	Quiet Series™
FAST®	SuperSOT™-3
FASTr™	SuperSOT™-6
GTO™	SuperSOT™-8
HiSeC™	TinyLogic™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Introduction

Power MOSFETs (Metal Oxide Semiconductor, Field Effect Transistors) differ from bipolar transistors in operating principles, specifications, and performance. In fact, the performance characteristics of MOSFETs are generally superior to those of bipolar transistors: significantly faster switching time, simpler drive circuitry, the absence of or reduction of the second-breakdown failure mechanism, the ability to be paralleled, and stable gain and response time over a wide temperature range. This note provides a basic explanation of general MOSFET characteristics, and a more thorough discussion of structure, thermal characteristics, gate parameters, operating frequency, output characteristics, and drive requirements.

General Characteristics

A conventional n-p-n bipolar power transistor is a current-driven device whose three terminals (base, emitter, and collector) are connected to the silicon by alloyed metal contacts. Bipolar transistors are described as minority-carrier devices in which injected minority carriers recombine with majority carriers. A drawback of recombination is that it limits the device's operating speed. And because of its current-driven base-emitter input, a bipolar transistor presents a low-impedance load to its driving circuit. In most power circuits, this low-impedance input requires somewhat complex drive circuitry.

By contrast, a power MOSFET is a voltage-driven device whose gate terminal, Figure 1(a), is electrically isolated from its silicon body by a thin layer of silicon dioxide (SiO_2). As a majority-carrier semiconductor, the MOSFET operates at much higher speed than its bipolar counterpart because there is no charge-storage mechanism. A positive voltage applied to the gate of an n-type MOSFET creates an electric field in the channel region beneath the gate; that is, the electric charge on the gate causes the p-region beneath the gate to convert to an n-type region, as shown in Figure 1(b). This conversion, called the surface-inversion phenomenon, allows current to flow between the drain and source through an n-type material. In effect, the MOSFET ceases to be an n-p-n device when in this state. The region between the drain and source can be represented as a resistor, although it does not behave linearly, as a conventional resistor would. Because of this surface-inversion phenomenon, then, the operation of a MOSFET is entirely different from that of a bipolar transistor, which always retain its n-p-n characteristic.

By virtue of its electrically-isolated gate, a MOSFET is described as a high-input impedance, voltage-controlled device, whereas a bipolar transistor is a low-input-impedance, current-controlled device. As a majority-carrier semiconductor, a MOSFET stores no charge, and so can switch faster than a bipolar device. Majority-carrier semiconductors also tend to slow down as temperature increases. This effect, brought about by another phenomenon called carrier mobility (where mobility

is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) makes a MOSFET more resistive at elevated temperatures, and much more immune to the thermal-runaway problem experienced by bipolar devices.

A useful by-product of the MOSFET process is the internal parasitic diode formed between source and drain, Figure 1(c). (There is no equivalent for this diode in a bipolar transistor other than in a bipolar darlington transistor.) Its characteristics make it useful as a clamp diode in inductive-load switching.

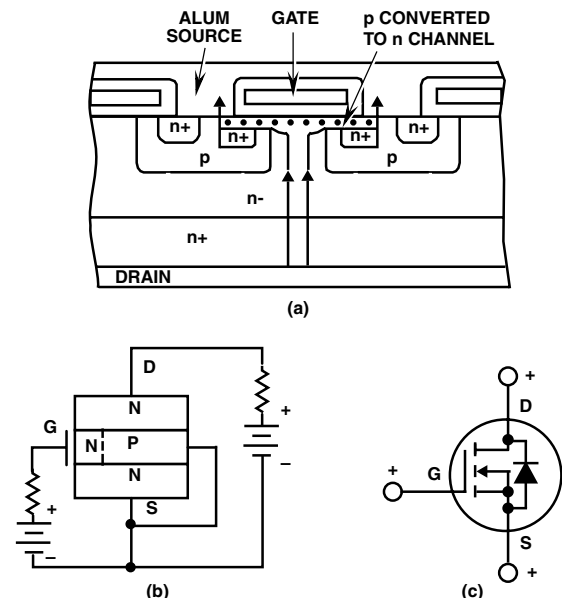


FIGURE 1. THE MOSFET, A VOLTAGE-CONTROLLED DEVICE WITH AN ELECTRICALLY ISOLATED GATE, USES MAJORITY CARRIERS TO MOVE CURRENT FROM SOURCE TO DRAIN (A). THE KEY TO MOSFET OPERATION IS THE CREATION OF THE INVERSION CHANNEL BENEATH THE GATE WHEN AN ELECTRIC CHARGE IS APPLIED TO THE GATE (B). BECAUSE OF THE MOSFET'S CONSTRUCTION, AN INTEGRAL DIODE IS FORMED ON THE DEVICE (C), AND THE DESIGNER CAN USE THIS DIODE FOR A NUMBER OF CIRCUIT FUNCTIONS

Structure

Intersil Power MOSFETs are manufactured using a vertical double-diffused process, called VDMOS or simply DMOS. A DMOS MOSFET is a single silicon chip structured with a large number of closely packed, hexagonal cells. The number of cell varies according to the dimensions of the chip. For example, a 120-mil² chip contains about 5,000 cells; a 240-mil² chip has more than 25,000 cells.

One of the aims of multiple-cells construction is to minimize the MOSFET parameter $r_{DS(ON)}$, or resistance from drain to source, when the device is in the on-state. When $r_{DS(ON)}$ is minimized, the device provides superior power-switching

Application Note 7500

performance because the voltage drop from drain to source is also minimized for a given value of drain-to-source current.

Since the path between drain and source is essentially resistive, because of the surface-inversion phenomenon, each cell in the device can be assumed to contribute an amount, R_N , to the total resistance. An individual cell has a fairly low resistance, but to minimize $r_{DS(ON)}$, it is necessary to put a large number of cells in parallel on a chip. In general, therefore, the greater the number of paralleled cells on a chip, the lower its $r_{DS(ON)}$ value:

$r_{DS(ON)} = R_N/N$, where N is the number of cells.

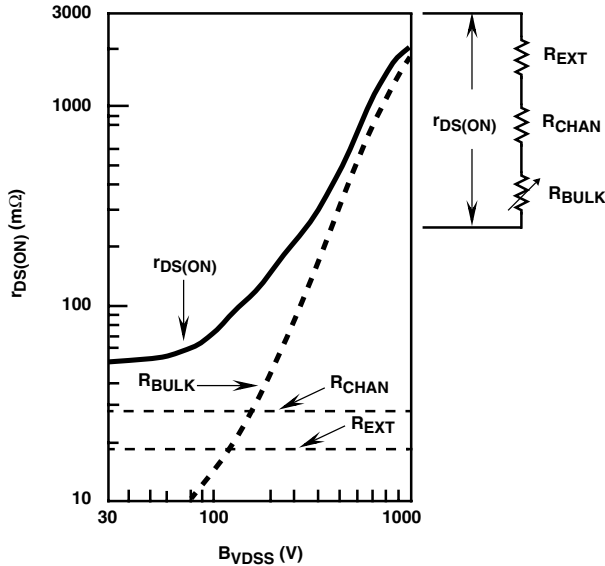


FIGURE 2. THE DRAIN-TO-SOURCE RESISTANCE, $r_{DS(ON)}$, OF A MOSFET IS NOT ONE BUT THREE SEPARATE RESISTANCE COMPONENTS

TABLE 1. PERCENTAGE RESISTANCE COMPONENTS FOR A TYPICAL CHIP

B_{VDSS}	40V	150V	500V
$R_{CHANNEL}$	50%	23%	2.4%
R_{BULK}	35%	70%	97%
$R_{EXTERNAL}$	15%	7%	<1%

In reality, $r_{DS(ON)}$ is composed of three separate resistances. Figure 2 shows a curve of the three resistive components for a single cell and their contributions to the overall value of $r_{DS(ON)}$. The value of $r_{DS(ON)}$ at any point of the curve is found by adding the values of the three components at that point:

$$r_{DS(ON)} = R_{BULK} + R_{CHAN} + R_{EXT}$$

where R_{CHAN} represents the resistance of the channel beneath the gate, and R_{EXT} includes all resistances resulting from the substrate, solder connections, leads, and the package. R_{BULK} represents the resistance resulting from the narrow neck of n material between the two layers, as shown in Figure 1(a), plus the resistance of the current path below the neck and through the body to the substrate region of the device.

Note in Figure 2 that R_{CHAN} and R_{EXT} are completely independent of voltage, while R_{BULK} is highly dependent on applied voltage. Note also that below about 150 volts, $r_{DS(ON)}$ is dominated by the sum of R_{CHAN} and R_{EXT} . Above 150 volts, $r_{DS(ON)}$ is increasingly dominated by R_{BULK} . Table 1 gives a percentage breakdown of the contribution of each resistance for three values of voltage.

Two conclusions, inherent consequences of the laws of semiconductor physics, and valid for any DMOS device, can be drawn from the preceding discussion: First, $r_{DS(ON)}$ obviously increases with increasing breakdown-voltage capability of a MOSFET. Second, minimum $r_{DS(ON)}$ performance must be sacrificed if the MOSFET must withstand ever-higher breakdown voltages.

The significance of R_{BULK} in devices with a high voltage capability is due to the fact that thick, lightly doped epi layers are required for the drain region in order to avoid producing high electric fields (and premature breakdown) within the device. And as the epi layers are made thicker and less resistive to support high voltages, the bulk component of resistance rapidly increases (see Figure 2) and begins to dominate the channel and external resistance. The $r_{DS(ON)}$ therefore, increases with increasing breakdown voltage capability, and low $r_{DS(ON)}$ must be sacrificed if the MOSFET is to withstand even higher breakdown voltages.

There is a way around these obstacles. The $r_{DS(ON)}$ in Figure 2 holds only for a given cell and chip size. Using a larger chip results in a lower value for $r_{DS(ON)}$ because a large chip has more cells (see Figure 3), shifting the vertical axis for each of the constituent parts.

The penalty for using a larger chip, however, is an increase in cost, since chip size is a major cost factor. And because chip area increases exponentially, not linearly, with voltage, the additional cost can be substantial. For example, to obtain a given $r_{DS(ON)}$ at a breakdown voltage twice as great as the original, the new chip requires an area four or five times larger than the original. Although the cost does not rise exponentially, it is substantially more than the original cost.

Effects of Temperature

The high operating temperatures of bipolar transistors are frequent cause of failure. The high temperatures are caused by hot-spotting, the tendency of current in a bipolar device to concentrate in areas around the emitter. Unchecked, this hot-spotting results in the mechanism of thermal runaway, and eventual destruction of the device. MOSFETs do not suffer this disadvantage because their current flow is in the form of majority carriers. The mobility of majority carriers (where, again, mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) is temperature dependent in silicon: mobility decreases with increasing temperature. This inverse relationship dictates that the carriers slowdown as the chip gets hotter. In effect, the resistance of the silicon path is increased, which prevents the concentrations of current that lead to hot spots. In fact, if hot spots do attempt to form in a MOSFET, the local resistance increases and defocuses or spreads out the current, rerouting it to cooler portions of the chip.

Application Note 7500

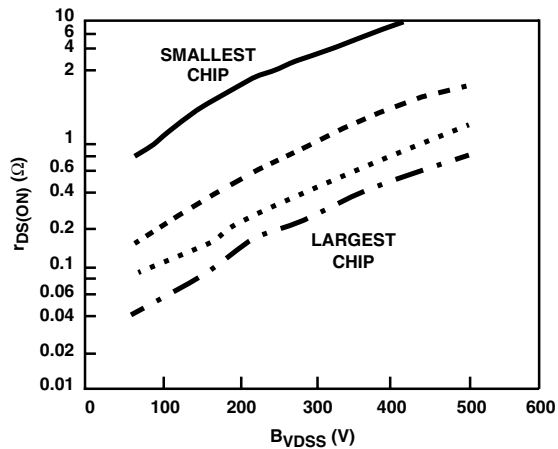


FIGURE 3. AS CHIP SIZE INCREASES, $r_{DS(ON)}$ DECREASES

Because of the character of its silicon structure, a MOSFET has a positive temperature coefficient of resistance, as shown by the curves of Figure 4.

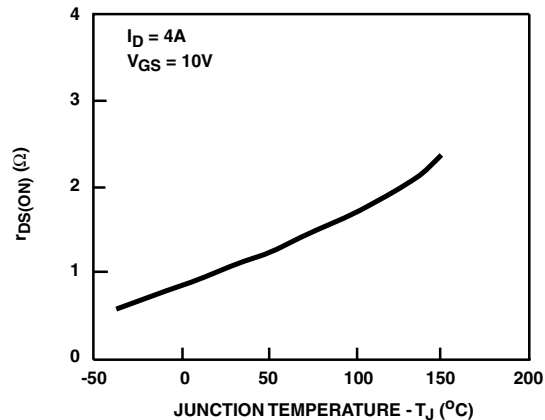


FIGURE 4. MOSFETs HAVE A POSITIVE TEMPERATURE COEFFICIENT OF RESISTANCE, WHICH GREATLY REDUCES THE POSSIBILITY OF THERMAL RUNAWAY AS TEMPERATURE INCREASES

The positive temperature coefficient of resistance means that a MOSFET is inherently more stable with temperature fluctuation, and provides its own protection against thermal runaway and second breakdown. Another benefit of this characteristic is that MOSFETs can be operated in parallel without fear that one device will rob current from the others. If any device begins to overheat, its resistance will increase, and its current will be directed away to cooler chips.

Gate Parameters

To permit the flow of drain-to-source current in an n-type MOSFET, a positive voltage must be applied between the gate and source terminals. Since, as described above, the gate is electrically isolated from the body of the device, theoretically no current can flow from the driving source into the gate. In reality, however, a very small current, in the

range of tens of nanoamperes, does flow, and is identified on data sheets as a leakage current, I_{GSS} . Because the gate current is so small, the input impedance of a MOSFET is extremely high (in the megohm range) and, in fact, is largely capacitive rather than resistive (because of the isolation of the gate terminal).

Figure 5 illustrates the basic input circuit of a MOSFET. The elements are equivalent, rather than physical, resistance, R , and capacitance, C . The capacitance, called C_{ISS} on MOSFET data sheets, is a combination of the device's internal gate-to-source and gate-to-drain capacitance. The resistance, R , represents the resistance of the material in the gate circuit. Together, the equivalent R and C of the input circuit will determine the upper frequency limit of MOSFET operation.

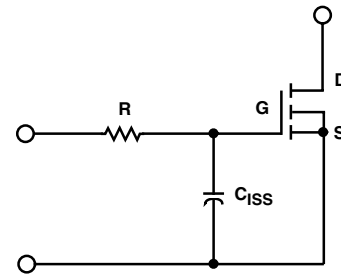


FIGURE 5. A MOSFETs SWITCHING SPEED IS DETERMINED BY ITS INPUT RESISTANCE R AND ITS INPUT CAPACITANCE C_{ISS}

Operating Frequency

Most DMOS processes use a polysilicon gate structure rather than the metal-gate type. If the resistance of the gate structure (R in Figure 5) is high, the switching time of the DMOS device is increased, thereby reducing its upper operating frequency. Compared to a metal gate, a polysilicon gate has a higher gate resistance. This property accounts for the frequent use of metal-gate MOSFETs in high-frequency (greater than 20MHz) applications, and polysilicon-gate MOSFETs in higher-power but lower-frequency systems.

Since the frequency response of a MOSFET is controlled by the effective R and C of its gate terminal, a rough estimate can be made of the upper operating frequency from datasheet parameters. The resistive portion depends on the sheet resistance of the polysilicon-gate overlay structure, a value of approximately 20 ohms. But whereas the total R value is not found on datasheets, the C value (C_{ISS}) is; it is recorded as both a maximum value and in graphical form as a function of drain-to-source voltage. The value of C_{ISS} is closely related to chip size; the larger the chip, the greater the value. Since the RC combination of the input circuit must be charged and discharged by the driving circuit, and since the capacitance dominates, larger chips will have slower switching times than smaller chips, and are, therefore, more useful in lower-frequency circuits. In general, the upper frequency limit of most power MOSFETs spans a fairly broad range, from 1MHz to 10MHz.

Output Characteristics

Probably the most used MOSFET graphical data is the output characteristics or a plot of drain-to-source current (I_{DS}) as a function of drain-to-source voltage (V_{DS}). A typical characteristic, shown in Figure 6, gives the drain current that flows at various V_{DS} values as a function of the gate-to-source voltage (V_{GS}). The curve is divided into two regions: a linear region in which V_{DS} is small and drain current increases linearly with drain voltage, and a saturated region in which increasing drain voltage has no effect on drain current (the device acts as a constant-current source). The current level at which the linear portion of the curve joins with the saturated portion is called the pinch-off region.

Drive Requirements

When considering the V_{GS} level required to operate a MOSFET, note from Figure 6, that the device is not turned on (no drain current flows) unless V_{GS} is greater than a certain level (called the threshold voltage). In other words, the threshold voltage must be exceeded before an appreciable increase in drain current can be expected. Generally V_{GS} for many types of DMOS devices is at least 2V. This is an important consideration when selecting devices or designing circuits to drive a MOSFET gate: the gate-drive circuit must provide at least the threshold-voltage level, but preferably, a much higher one.

As Figure 6 shows, a MOSFET must be driven by a fairly high voltage, on the order of 10V, to ensure maximum saturated drain-current flow. However, integrated circuits, such as TTL types, cannot deliver the necessary voltage levels unless they are modified with external pull-up resistors. Even with a pull-up to 5V, a TTL driver cannot fully saturate most MOSFETs. Thus, TTL drivers are most suitable when the current to be switched is far less than the rated current of the MOSFET. CMOS ICs can run from supplies of 10V, and these devices are capable of driving a MOSFET into full saturation. On the other hand, a CMOS driver will not switch the MOSFET gate circuit as fast as a TTL driver. The best results, whether TTL or CMOS ICs provide the drive, are achieved when special buffering chips are inserted between the IC output and gate input to match the needs of the MOSFET gate.

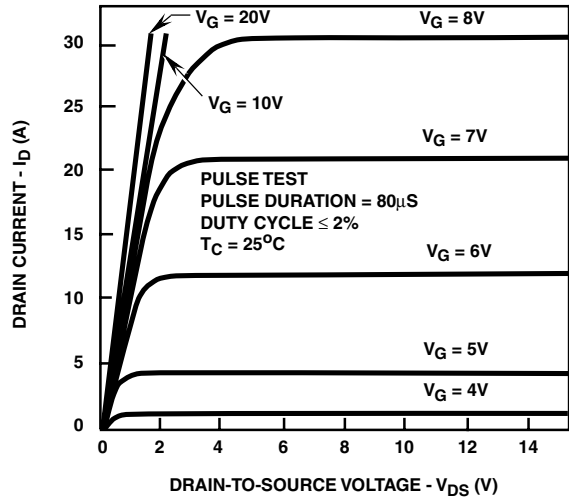


FIGURE 6. MOSFETs REQUIRE A HIGH INPUT VOLTAGE (AT LEAST 10V) IN ORDER TO DELIVER THEIR FULL RATED DRAIN CURRENT

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE _x TM	FAST [®]	PACMAN TM	SuperSOT TM -3
Bottomless TM	FAST _r TM	POP TM	SuperSOT TM -6
CoolFET TM	GlobalOptoisolator TM	PowerTrench [®]	SuperSOT TM -8
CROSSVOLT TM	GTO TM	QFET TM	SyncFET TM
DenseTrench TM	HiSeC TM	QS TM	TinyLogic TM
DOMET TM	ISOPLANAR TM	QT Optoelectronics TM	UHC TM
EcoSPARK TM	LittleFET TM	Quiet Series TM	UltraFET TM
E ² CMOS TM	MicroFET TM	SILENT SWITCHER [®]	VCX TM
EnSigna TM	MICROWIRE TM	SMART START TM	
FACT TM	OPTOLOGIC TM	Star* Power TM	
FACT Quiet Series TM	OPTOPLANAR TM	Stealth TM	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

The Do's and Don'ts of Using MOS-Gated Transistors (HEXFET® is the trademark for International Rectifier Power MOSFETs)

In this application note, some of the most common do's and don'ts of using power HEXFET®s are described. The objective is to help the user get the most out of these remarkable devices, while reducing "on the job" learning time to a minimum.

Topics Covered:

- Be Mindful of the Reverse Blocking Characteristics of the Device*
- Be Careful When Handling and Testing Power HEXFET®s*
- Beware of Unexpected Gate-to-Source Voltage Spikes*
- Beware of Drain or Collector Voltage Spikes Induced by Switching*
- Do Not Exceed the Peak Current Rating*
- Stay within the Thermal Limits of the Device*
- Pay Attention to Circuit Layout*
- Be Careful When Using the Integral Body-Drain Diode*
- Be On Your Gaurd When Comparing Current Ratings*

1. BE MINDFUL OF THE REVERSE BLOCKING CHARACTERISTICS OF THE DEVICE

IGBTs have a limited reverse blocking capability of approximately 20-30 V, with high leakage. This is characterized in IR's data sheets with a Reverse Avalanche Energy (E_{ARV}). This rating is useful to absorb energy spikes due to the stray inductance in series with the anti-parallel diode. This is a significant advantage over bipolar transistors and power darlingtonts. A feature of power MOSFETs is that they inherently have built into them an integral reverse body-drain diode. The existence of this diode is explained by reference to Figure 1. When the source terminal is made positive with respect to the drain, current can flow through the middle of the source cell, across a forward biased P-N junction. In the "reverse" direction, the power HEXFET® thus behaves like a P-N junction rectifier. The integral body-drain diode is a real circuit element, and its current handling capability is typically as high as that of the transistor itself. Some circuits require an "inverse" rectifier to be connected across the switching device, and in these circuits it will often be possible to utilize the body-drain diode of the HEXFET® provided the proper precautions are taken.

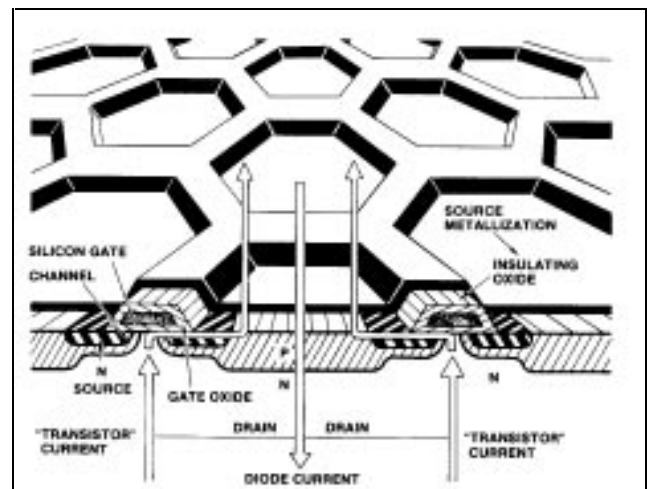


Figure 1. Basic HEXFET Structure

2. BE CAREFUL WHEN HANDLING & TESTING POWER HEXFET®S

The user's first "contact" with a MOS-gated transistor could be a package of parts arriving on his desk. Even at this stage, it behooves one to be knowledgeable about some elementary precautions. Being MOS devices, HEXFET®s can be damaged by static charge when handling, testing or installing into a circuit. Power Devices have large input capacitance, and are able to absorb static charge without excessive buildup of voltage. In order to avoid possible problems, however, the following procedures should be followed as a matter of good practice, wherever possible:

- MOS-gated transistors should be left in their anti-static shipping bags, or conductive foam, or they should be placed in metal containers or conductive tote bins, until required for testing or connection into a circuit. The person handling the device should ideally be grounded through a suitable wrist strap, though in reality this added precaution is seldom essential.
- Devices should be handled by the package, not by the leads. When checking the electrical characteristics of the MOS-gated transistors on a curve tracer, or in a test circuit, the following precautions should be observed:
- Test stations should use electrically conductive floor and table mats that are grounded. Suitable mats are available commercially.

- When inserting the device in a curve tracer or a test circuit, voltage should not be applied until all terminals are solidly connected into the circuit.
- When using a curve tracer, a resistor should be connected in series with the gate to damp spurious oscillations that can otherwise occur on the trace. A suitable value of resistance is 100 ohms.
- For repeated testing, it is convenient to build this resistor into the test fixture.
- When switching from one test range to another, voltage and current settings should be reduced to zero, to avoid the generation of potentially destructive voltage surges during switching.

The next step is to connect the device into an actual circuit. The following simple precautions should be observed:

- Work stations should use electrically grounded table and floor mats.
- Soldering irons *should be grounded*.

Now that the device has been connected into its circuit, it is ready for the power to be applied. From here on, success in applying the device becomes a matter of the integrity of the circuit design, and of what circuit precautions have been taken to guard against unintentional abuse of its ratings.

The following are the interrelated device and circuit considerations that lead to reliable, trouble-free design.

3. BEWARE OF UNEXPECTED GATE-TO-SOURCE VOLTAGE SPIKES

Excessive voltage will punch through the gate-source oxide layer and result in permanent damage. This seems obvious enough, but it is not so obvious that transient gate-to-source overvoltages can be generated that are quite unrelated to, and well in excess of, the amplitude of the applied drive signal. The problem is illustrated by reference to Figure 2.

If we assume that the impedance, Z , of the drive source is high, then any positive-going change of voltage applied across the drain and source terminals (caused, for example, by the switching of another device in the circuit) will be reflected as a positive-going voltage transient across the source and the drain terminals, in the approximate ratio of:

$$\frac{1}{1 + \frac{C_{gs}}{C_{dg}}}$$

The above ratio is typically about 1 to 6. This means that a change of drain-to-source voltage of 300V, for example, could produce a voltage transient approaching 50V between the gate and source terminals. In practice this “aiming” voltage will not appear on the gate if the dv/dt is positive because the MOS-gated device goes in conduction at approximately $V_{gs} = 4V$, thereby clamping the dv/dt at the expense of a current transient and increased power dissipation. However, a negative-going dv/dt will not be clamped. This calculation is based upon the worst case assumption that the transient impedance of the drive circuit is high by comparison with the gate-to-source capacitance of the device. This situation can, in fact, be quite easily approximated if the gate drive circuit contains inductance—for example the leakage inductance of an isolating drive transformer. This inductance exhibits a high impedance for short transients, and effectively decouples the gate from its drive circuit for the duration of the transient.

The negative-going gate-to-source voltage transient produced under the above circumstances may exceed the gate voltage rating of the device, causing permanent damage. It is, of course, true that since the applied drain transient results in a voltage at the gate which tends to turn the device ON, the overall effect is to an extent self-limiting so far as the gate voltage transient is concerned. Whether this self-limiting action will prevent the voltage transient at the gate from exceeding the gate-source voltage rating of the device depends upon the impedance of the external circuit. Spurious turn-on is of itself undesirable, of course, though in practical terms one may grudgingly be able to accept this circuit operating imperfection, provided the safe operating area of the device is not violated.

Notice that a voltage clamp (a conventional zener diode is suitable for this purpose) to prevent the gate-source voltage rating from being exceeded will not prevent the dv/dt induced turn-on, as the gate will not reach the zener voltage. In many instances the zener is responsible for generating oscillations in the gate circuit, particularly when a significant amount of stray inductance is present. A more fundamental solution, of course, is to make the impedance of the gate circuit low enough that not only is the gate-source voltage rating not exceeded, but also the voltage transient at the gate is contained to a level at which spurious turn-on does not occur.

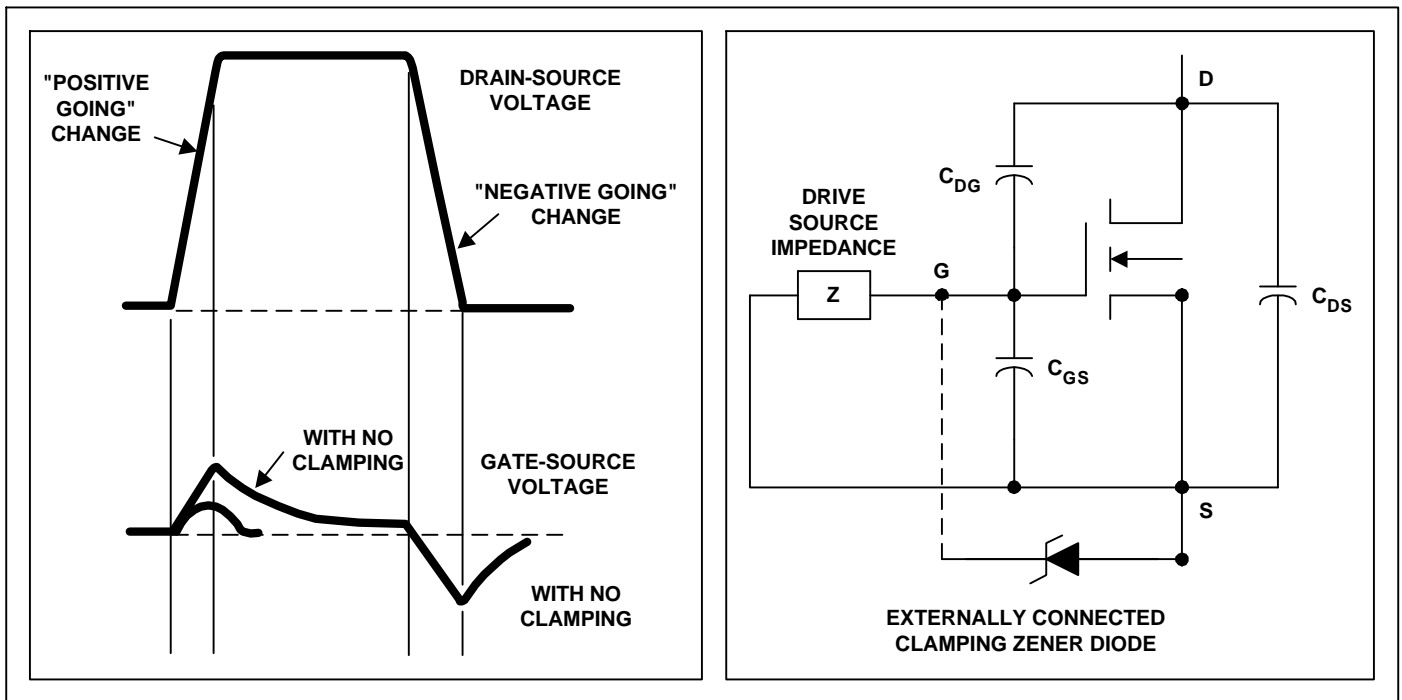


Figure 2. A Rapidly Changing Applied Drain-Source Voltage will Produce Gate-Source Transients

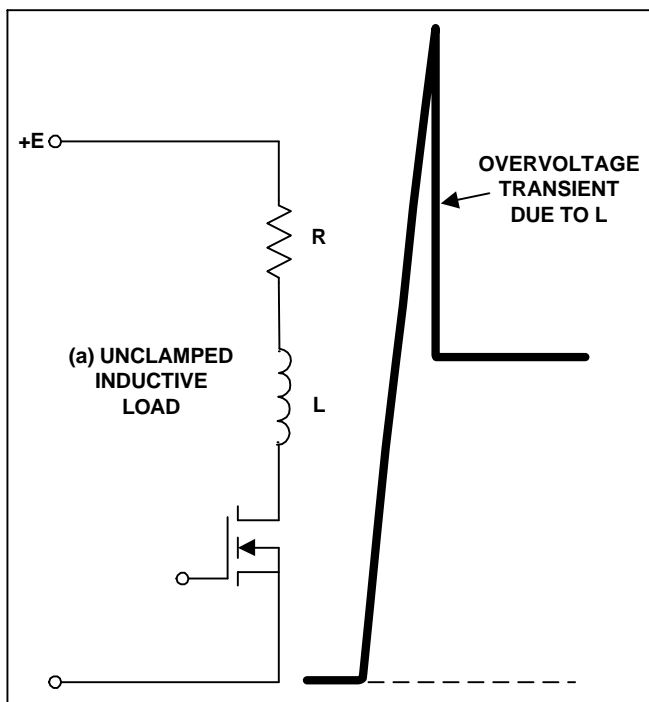


Figure 3. Drain-Source Overvoltage Transient when Switching Off with Unclamped Inductive Load

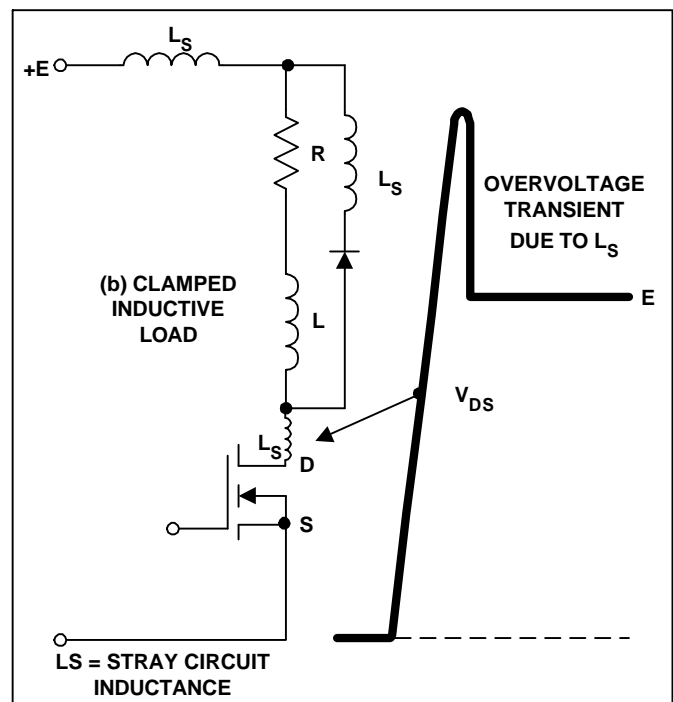


Figure 4. Drain-Source Overvoltage Transient Produced by Stray Circuit Inductance When Switching Off with Clamped, Inductive Load

It should be remembered that a collapse of voltage across the device (i.e., a negative-going dv/dt) will produce a transient negative voltage spike across the gate-source terminals. In this case, of course, there will be no tendency for the device to turn ON, and hence no tendency for the effect to be self-limiting. A zener diode connected to clamp positive transients will automatically clamp negative-going transients, limiting them to the forward conduction voltage drop of the zener.

4. BEWARE OF DRAIN OR COLLECTOR VOLTAGE SPIKES INDUCED BY SWITCHING

The uninitiated designer is often not aware that self-inflicted overvoltage transients can be produced when the device is switched OFF, even though the DC supply voltage for the drain circuit is well below the V_{DS} rating of the transistor.

Figure 3 shows how a voltage spike is produced when switching the device OFF, as a result of inductance in the circuit. The faster the device is switched, the higher the overvoltage will be.

Inductance is always present to some extent in a practical circuit, and therefore, there is always danger of inducing overvoltage transients when switching OFF. Usually, of course, the main inductive component of the load will be "clamped", as shown in Figure 4. Stray circuit inductance still exists, however, and overvoltage transients will still be produced as a result—to say nothing of the fact that the clamping diode may not provide an instantaneous clamping action, due to its "forward recovery" characteristic.

The first approach to this problem is to minimize stray circuit inductance, by means of careful attention to circuit layout, to the point that whatever residual inductance is left in the circuit can be tolerated. HEXFET[®]s have an inductive energy rating that makes capable of withstanding these inductive spikes, assuming that the data sheet limits for energy and temperature are not violated. IGBTs, however, do not have an avalanche rating, and a clamping device should be connected, physically as close as possible to the drain and source terminals, as shown in Figure 5. A conventional zener diode, or a "transorb" clamping device, are satisfactory for this purpose. An alternative clamping circuit is shown in Figure 6, depending on the voltage and current rating of the circuit.

The capacitor C is a reservoir capacitor and charges to a substantially constant voltage, while the resistor R is sized to dissipate the "clamping energy" while maintaining the desired voltage across the capacitor. The diode D must be chosen so that its forward recovery characteristic does not significantly spoil the transient clamping action of the circuit. A simple RC snubber can also be used, as shown in Figure 7. Note, however, that an RC snubber not only limits the peak voltage, it also slows down the effective switching speed. In so doing, it absorbs energy during the whole of the switching period, not just at the end of it, as does a voltage clamp. A snubber is therefore less efficient than a true voltage clamping device.

Note that the highest voltage transient occurs when switching the highest level of current. The waveform of the voltage across the device should be checked with a high-speed oscilloscope at the full load condition to ensure that switching voltage transients are within safe limits.

5. DO NOT EXCEED THE PEAK CURRENT RATING

All power transistors have a specified maximum peak current rating. This is conservatively set at a level that guarantees reliable operation and it should not be exceeded. It is often overlooked that, in a practical circuit, peak transient currents can be obtained that are well in excess of the expected normal operating current, unless proper precautions are taken. Heating, lighting and motor loads, for example, consume high in-rush currents if not properly controlled. A technique that ensures that the peak current does not exceed the capability of the device is to use a current sensing control that switches it OFF whenever the current instantaneously reaches a preset limit.

Unexpectedly high transient current can also be obtained as a result of rectifier reverse recovery, when a transistor is switched ON rapidly into a conducting rectifier. This is illustrated in Figure 8. The solution is to use a faster rectifier, or to slow down the switching of the transistor to limit the peak reverse recovery current of the rectifier.

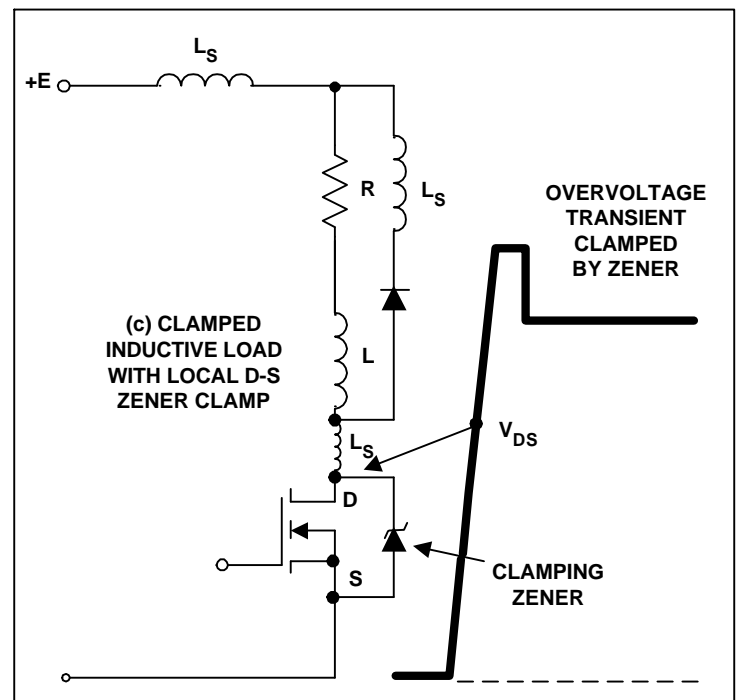


Figure 5. Overvoltage Transient at Switch-Off Clamped by Local Drain-Source Zener

6. STAY WITHIN THE THERMAL LIMITS

Power transistors are thermally limited. They must be mounted on a heatsink that is adequate to keep the junction temperature within the rated under the "worst case" condition of maximum power dissipation and maximum ambient temperature.

It must be remembered that in a switching application, the total power is due to the conduction losses and the switching loss. Switching time and switching losses of HEXFET®s are essentially independent of temperature, but the conduction losses increase with increasing temperature, because $R_{DS(on)}$ increases with temperature. IGBTs, on the contrary, have switching losses that highly dependent of temperature, while conduction losses are not. This must be taken into account when sizing the heatsink. The required thermal resistance of the heatsink can be calculated as follows:

The transistor conduction power, P_T , is given approximately by $P_T = \text{On-state Voltage} \times \text{Drain or Collector current}$

The switching energy depends upon the voltage and current being switched and the type of load. The total switching loss, P_S , is the total switching energy, ϵ_T , multiplied by the operating frequency, f . ϵ_T is the sum of the energies due to the individual switchings that take place in each fundamental operating cycle:

$$P_S = \epsilon_T f$$

The total power dissipation is the sum of the conduction power, P_T , and the switching power, P_S .

$$P = P_T + P_S$$

Since:

$$\Delta T_{JA} = PR_{th}$$

where:

R_{th} = junction-to-ambient thermal resistance

The junction-to-ambient thermal resistance, R_{JA} , is made up of the internal junction-to-case thermal resistance, R_{JC} , plus the case-to-heatsink thermal resistance, R_{CS} , plus the sink-to-ambient thermal resistance, R_{SA} . The first two terms are fixed for the device, and the required thermal resistance of the heatsink, R_{SA} , for a given junction temperature rise ΔT_{J-A} , can be calculated from:

$$R_{S-A} = R_{J-A} - (R_{JC} + R_{C-S})$$

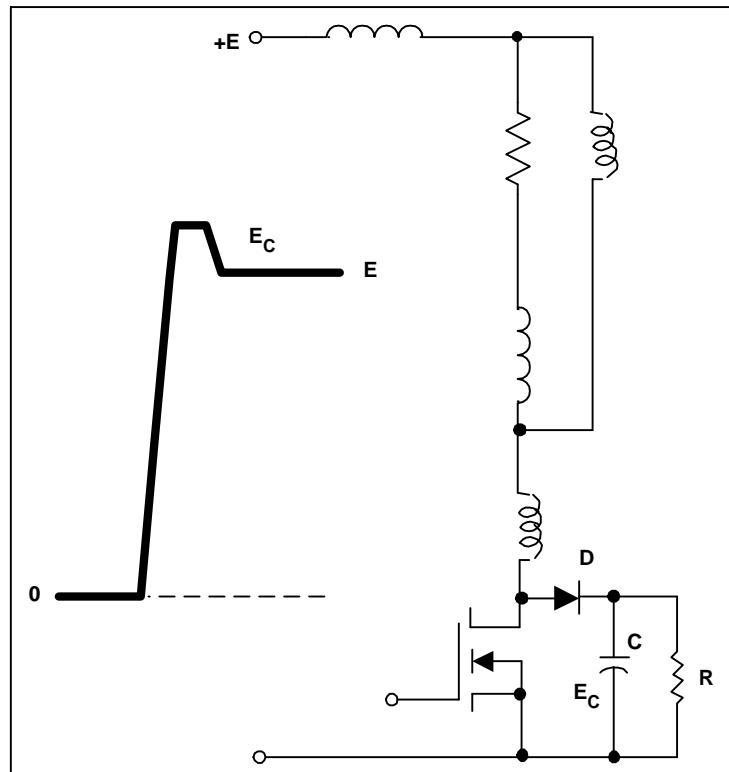


Figure 6. Overvoltage Transient at Switch-Off Limited by Local Clamp

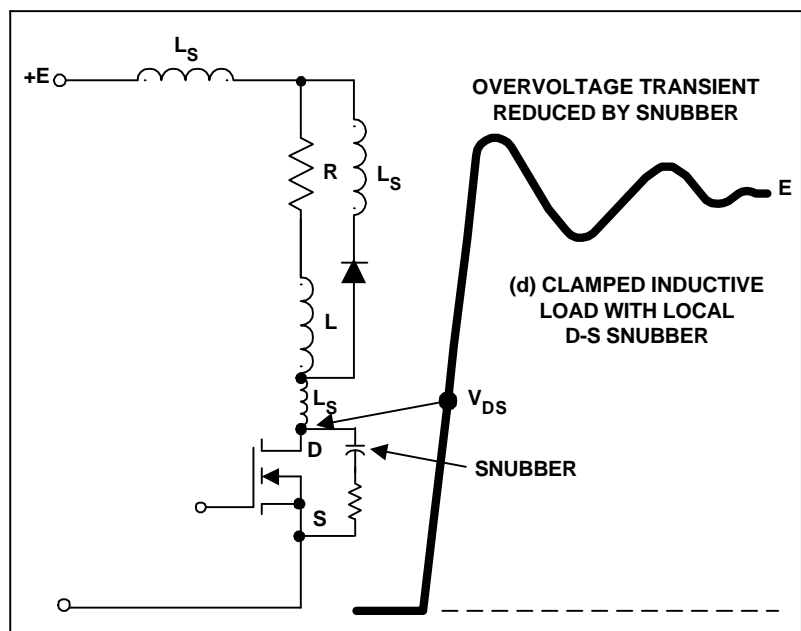


Figure 7. Overvoltage Transient at Switch-Off Limited by Local Capacitor-Resistor Snubber

7. PAY ATTENTION TO CIRCUIT LAYOUT

Stray inductance in the circuit can cause overvoltage transients, slowing down of the switching speed, unexpected unbalance of current between parallel connected devices, and unwanted oscillations.

In order to minimize these effects, stray circuit inductance must be minimized. This is done by keeping conduction paths as short as possible, by minimizing the area of current loops, by using twisted pairs of leads, and by using ground plane construction. Local decoupling capacitors alleviate the affects of any residual circuit inductance, once these measures have been taken. Circuit layout should be kept as symmetrical as possible in order to maintain balanced currents in parallel connected HEXFET[®]s or IGBTs. The gates of parallel connected devices should be decoupled by small ferrite beads placed over the gate connections, or by individual resistors in series with each gate. These measures prevent parasitic oscillations.

8. BE CAREFUL WHEN USING THE INTEGRAL BODY-DRAIN DIODE

The HEXFET[®]s integral body-drain diode exhibits minority carrier reverse recovery. Reverse recovery presents a potential problem when switching any rectifier off; the slower the rectifier, the greater the problem. By comparison with the HEXFET[®] itself, the switching speed of the integral reverse rectifier is quite slow. The switching speed of a circuit which utilizes the body-drain diode of the HEXFET[®] may therefore be limited by the rectifier. Whether this will be so depends upon the circuit and the operating conditions.

Regardless of the overall circuit configuration, or the particular application, the "local" circuit operating situation that is troublesome occurs when the freewheeling current from an inductive load is commutated from the integral rectifier of one HEXFET[®] to the transistor of an "opposite" HEXFET[®], the two devices forming a tandem series connected pair across a low impedance voltage source, as shown in Figure 8. This "local" circuit configuration occurs in most chopper and inverter schemes.

If the incoming HEXFET[®] switches ON too rapidly, the peak reverse recovery current of the integral body-drain diode of the opposite HEXFET[®] will rise too rapidly, the peak reverse recovery current rating will be exceeded, and the device may possibly be destroyed.

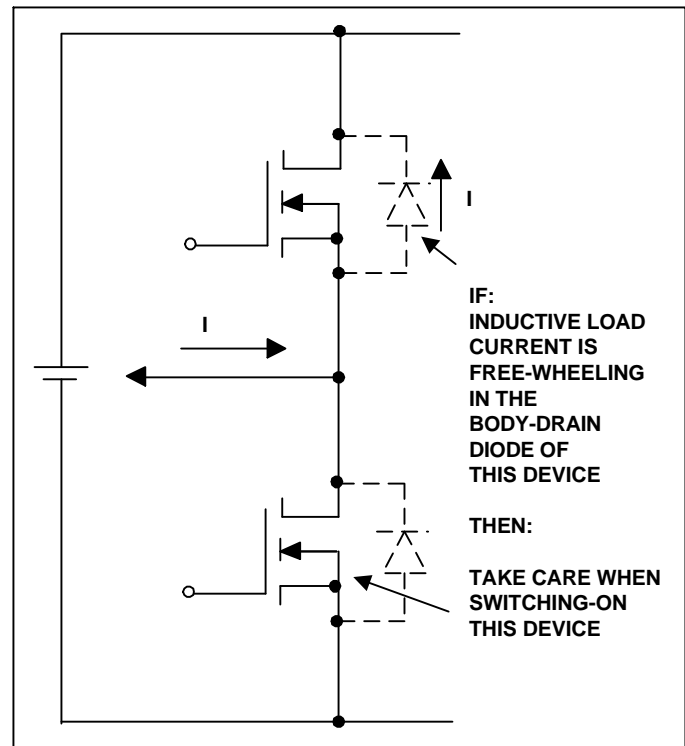


Figure 8. Local Circuit Configuration and Operating Condition Requiring Special Care When Using the HEXFET's Integral Body-Drain Diode.

The peak reverse recovery current of the rectifier can be reduced by slowing down the rate of change of current during the commutation process. The rate of change of current can be controlled by purposefully slowing down the rate of rise of the gate driving pulse. Using this technique, the peak current can be reduced to almost any desired extent, at the expense of prolonging the high dissipation switching period.

The oscillograms in Figure 9 illustrate the effect. By slowing the total switch-ON time from 300ns to 1.8ms, the peak current of the IRF330 has been decreased from 20A to 10A. The energy dissipation associated with the "unrestrained" switch-ON in Figure 9(a) is 0.9mJ, whereas it is 2.7mJ for the controlled switch-ON of Figure 9(b).

Note also that it is not necessary to slow the switching-OFF of the HEXFET[®], hence the energy dissipation at switch-OFF will be relatively small by comparison with that at switch-ON. For operation at frequencies up to a few kHz, where ultra-fast switching is not mandatory, slowing the applied gate drive signal to reduce the peak reverse recovery current of the "opposite" rectifier offers a good practical solution.

9. BE ON YOUR GUARD WHEN COMPARING CURRENT RATINGS

The user can be forgiven if he assumes that the continuous drain current rating, that appears on the data sheet represents the current at which the device can actually be operated continuously in a practical system. To be sure, that's what it should represent; unfortunately it often does not.

Frequently a "continuous" current rating is assigned to the device which in practical terms cannot be used, because the resulting conduction power dissipation would be so large as to require a heatsink with an impractically low thermal resistance, and/or an impractically low ambient operating temperature. The best advice to the user is to compare different types *on the basis of high temperature conduction and switching losses*, and not of current rating. For MOSFETS, it is sufficient to compare $R_{DS(on)}$ at 25° C, and this provides a common basis for comparison. This parameter, taken in conjunction with the junction-case thermal resistance, is a much better indication of the power MOSFET true current handling capability.

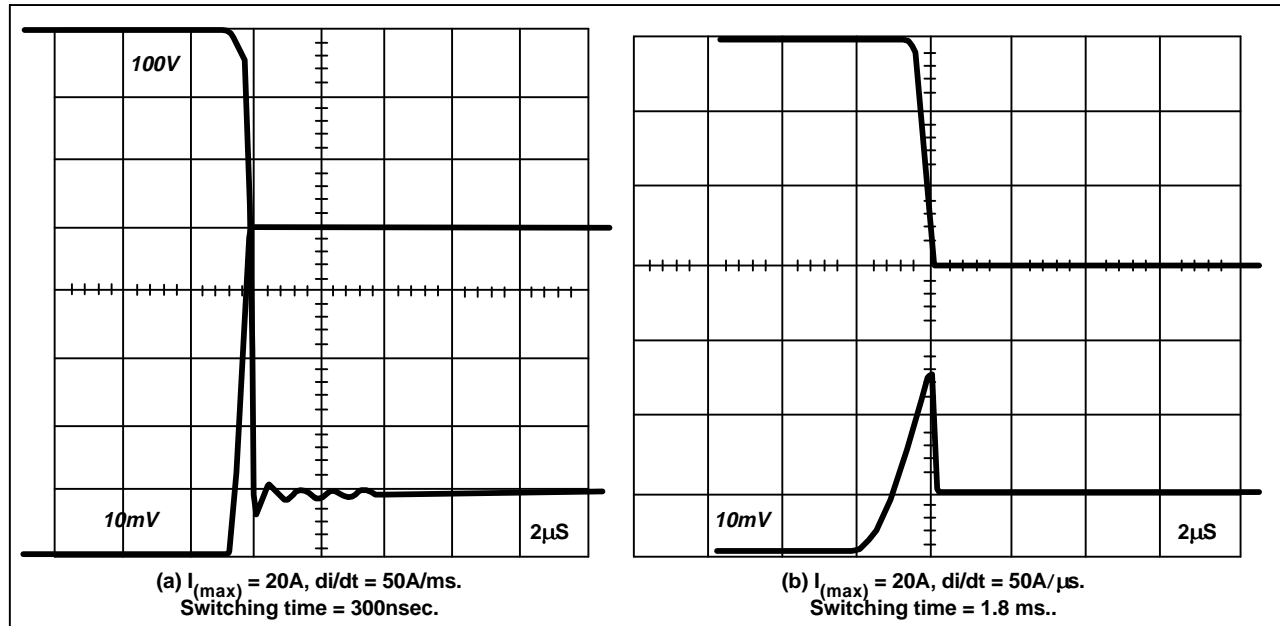


Figure 9. Oscillograms of IRF330 Switching into Reverse Rectifier of Another IRF330 with Freewheeling Current of 4A.

Top Trace: Voltage 100V/div.
Bottom Trace: Current 4A/div.
Time Scale: 2ms/div.

Current Ratings of Power Semiconductors

<http://www.irf.com/technical-info/appnotes/an-949.pdf>

Topics Covered:

What is a current rating?
Current ratings for power semiconductors
Continuous current ratings
Current ratings under duty cycle conditions
Transient thermal impedance
Peak Current Ratings of Power Semiconductors
RMS values of common waveforms

1. WHAT IS A CURRENT RATING?

The current rating of an electrical device, be that a circuit breaker or a motor or a transformer, is the current at which the temperature within the electrical device reaches a value that may impair the reliability or functionality of the device itself. The manufacturer knows the temperature limits of the materials used in the device, but he does not know the temperature of the ambient in which the device will be used. So he makes an assumption on this temperature. This has two important consequences:

1. **A current rating is meaningless without the rated temperature**
2. **The temperature at which the rating applies may, or may not be related to actual operating conditions.** If it is, the current rating can be used as **an indication** of the current capability of that device in a real applications. If the device is rated at a temperature that is not encountered in a typical operating environment, e.g. 25°C, **it cannot be trusted to provide an indication of actual device capability in an application.** It can only be used to compare the ratings of similar devices rated at the same temperature.

The rating of electrical devices like motors and circuit breakers are dictated by various agreements and regulations. The ratings of many other devices, like transformers, resistors and semiconductors are specified in their data sheets. As a result, the user must do, *at a minimum*, a verification that the device is capable of operating:

- a) at the maximum current
- b) at the maximum ambient temperature
- c) without exceeding its maximum temperature

2. CURRENT RATINGS FOR POWER SEMICONDUCTORS

Like any other electrical device, power semiconductors must be operated within their maximum temperature. Since the vast majority of power semiconductors operate at large power densities, they need to be heatsunk. It is the task of the designer to identify the heatsink, or other cooling method, that fulfills the requirements a, b and c of the previous section. This task is normally referred to as “thermal design”.

Power semiconductors have, however, some additional limitations normally associated with their capability of handling high voltages and high currents at the same time, under static or dynamic conditions. These limitations are peculiar to the specific type of semiconductor, e.g. SOA for transistors, dv/dt , di/dt and t_q for thyristors, t_{tr} for diodes. Information on these limitations are normally contained in publications that are specific to the particular device.

Bipolar transistors have one additional limitation that is not common to other power semiconductors: gain. To operate a bipolar transistor at its headlined “rated” continuous current would require an inconveniently large amount of drive current, and the saturation voltage and switching times would be hard to live with in a practical design.

Other power semiconductors are not limited by gain. IGBT for motor drive applications are, by design, limited in gain to current levels much beyond normal operating conditions to reduce the current under short-circuit conditions.

3. CONTINUOUS CURRENT RATINGS

The continuous rating of a power semiconductor is based on *heat removal when conducting a fixed amount of current*. This is determined by the fundamental equation for temperature rise (see INT-936), with no switching losses present. Rated I_D , for a MOSFET is therefore:

$$I_D = \sqrt{\frac{T_{JMAX} - T_C}{R_{DS(on)} R_{th(JC)}}}$$

where $R_{DS(on)}$ is the limiting value of the on-resistance *at rated T_{Jmax} , at the appropriate value of I_D* . $R_{th(JC)}$ is the maximum value of internal junction-to-case thermal resistance, and T_c is the case temperature.

Similarly, the continuous current rating of a diode, or a thyristor, or an IGBT is calculated from the basic equation of temperature rise. The power dissipation is calculated from voltage drop and continuous current.

Except for water-cooled sinks, it is very difficult to keep the case temperature of a power semiconductor at less than 90°. Thus, the usable *continuous direct* current of a power device for most practical is whatever is applicable to a case temperature of 90 to 110° C. This allows a sufficient differential between case and ambient temperature for the heat dissipator to handle the heat transfer.

The “headlined” continuous current rating shown on the data sheets of most power transistors is usually larger than the above practically usable level of *continuous* drain current. This is because the case temperature adopted by the industry, to which the “headlined” continuous I_D rating applies, is 25°C.

Figure 1 shows typical heatsinks for TO-3 and TO-220 packaged HEXFET®s that allow them to operate in a 40°C ambient at a *continuous direct* drain current that is 60 to 70% of the rated continuous drain current at $T_c = 25^\circ\text{C}$; the corresponding *steady* case temperature is about 100°C.

The continuous current rating of power transistors is, however, of little direct use to the designer, other than as a benchmark, for the following three reasons:

1. Power transistors are normally operated in switchmode, with duty cycles considerably less than 100%, and what is really of interest is the current-carrying capability of the device under the actual “switched” operating conditions.
2. When operated in switchmode, power transistors have switching losses, that have to be calculated and added to the conduction losses, as indicated in INT-936.
3. The selection of the power device may be dictated by surge requirements that make the continuous current rating irrelevant.

And, if this were not enough, advances in the low-voltage MOSFET technology have reduced conduction losses to the point that the package has become the limiting factor in their continuous current rating. This is explained in INTDT93-4

4. SWITCHING “DUTY CYCLE” RATINGS

The basic thermal equation of INT-936 determines the basic rating of a “thermal system” in a practical application. This equation can be used to determine how much power can be dissipated by a (known) thermal system or the junction temperature for a given set of electrical operating conditions (power dissipation). Since the power entered in that equation is the “average” power, it remains valid as long as the frequency of operation is high with respect to the thermal inertia of the system. When the frequency is very low (tens of Hz), the transient thermal response curve is used, as described below in Section 5.

The power dissipation is normally divided in conduction and switching. Conduction losses in a power MOSFET, being resistive in nature, can be calculated as $(I_{RMS})^2 \times R$. The RMS content of waveforms of different shape can be found in the Appendix. Switching losses can be calculated from the switching waveforms, from the gate charge or from analytical methods. Conduction and switching losses for IGBTs are more complex, as explained in INT-990.

5. JUNCTION TEMPERATURE UNDER PULSED CONDITIONS

Under surge conditions the junction temperature rises exponentially, according to its thermal inertia. Rather than using the thermal resistance, that is appropriate for steady state operation, we use the Transient Thermal Impedance (or, more correctly, Thermal Response Curve), as the one shown in Figure 2. For a surge of given duration (x axis), this curve gives a thermal response factor (y axis). The peak junction temperature due to the surge condition can be calculated as indicated in the figure itself. The power dissipation is normally calculated from the voltage and current across the device during the surge.

This curve is also useful for determining the peak junction temperature for power or pulses with a very low repetition rate, when the method described in the previous section is not applicable. The reason for this is illustrated by the waveforms in Figures 3(a) and 3(b). Both sets of waveforms are for the same power dissipation and duty cycle, but for different operating frequencies. The cycle-by-cycle fluctuations of junction temperature at 20Hz (Figure 3a) are clearly greater than at 200Hz (Figure 3b). As frequency increases, thermal inertia of the junction “irons out” instantaneous temperature fluctuations, and the junction responds more to average, rather than peak power dissipation. At frequencies above a few kHz and duty cycles above 20% or so, cycle-by-cycle temperature fluctuations become small, and peak junction temperature rise becomes equal to the average power dissipation multiplied by the DC junction-to-case thermal resistance, within one or two percent.

For pulses with low repetition rate the remaining curves in Figure 2 show effective thermal impedance at different duty cycles. These curves are approximately related to the single pulse curve, by the following relationship:

Effective normalized thermal impedance = $D + (1 - D) \times$ (transient thermal impedance for single pulse of duration t).

The thermal impedance, when multiplied by the power dissipation *during the conduction period t* (i.e., the power *within* the conduction pulse itself, *not* the power averaged over the whole cycle), gives the value of the repetitive peak junction-to-case temperature rise.

To determine the absolute value of the peak junction temperature, it is, of course, necessary to know the case temperature T_C under steady-state operating conditions. Because of thermal inertia, the heatsink responds only to average power dissipation (except at extremely low frequencies which generally will not be of practical interest). T_C is therefore given by:

$$T_C = T_A + (R_{thC-S} + R_{thS-A}) P_{AV}$$

where:

T_A = ambient temperature

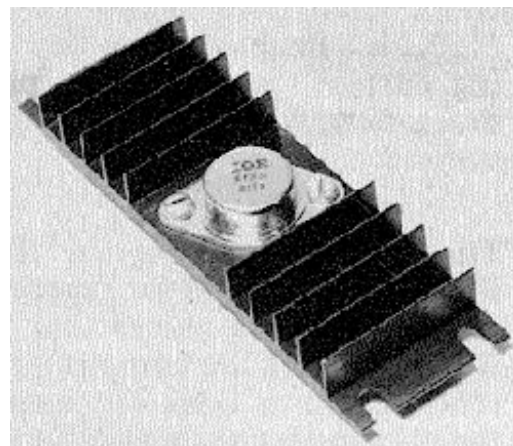
R_{thC-S} = case-to-sink thermal resistance

R_{thS-A} = sink-to-ambient thermal resistance

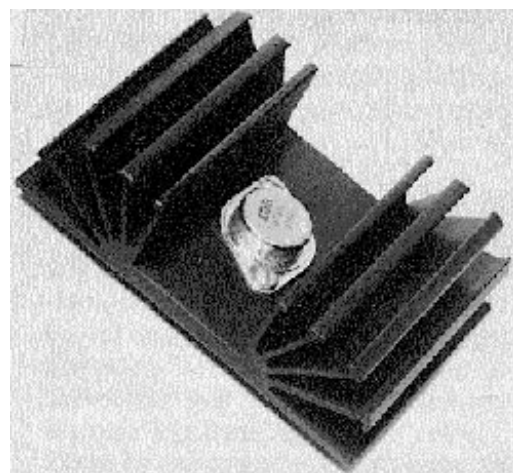
P_{AV} = average power dissipation

also,

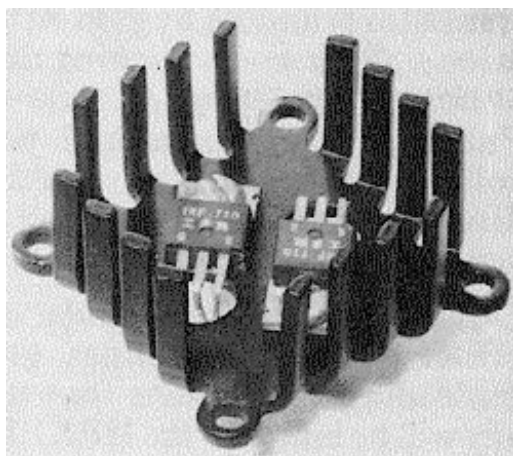
P_{AV} = peak power x duty cycle for rectangular pulses of power



(a) Type 621-A heatsink give 4A continuous rating for IRF331 with 5 CFM airflow in 40°C ambient.



(b) Type 641-A heatsink gives 3.5A continuous rating for IRF331 with natural convection cooling in 40°C ambient.



(c) Type 689-75 e4 heatsink give 1A continuous rating for IRF710 with natural convection cooling in 40°C ambient.

Figure 1. Typical Heatsinks for HEXFETs (Heatsink by Wakefield)

The transient thermal response curve *assumes constant case temperature*. This is generally valid for pulses shorter than 10ms. For longer surges the case temperature starts to rise and the results are of questionable accuracy. For operation in free air, case temperature starts to rise within few ms and this curve does not provide any useful information. More sophisticated analytical methods that take the entire thermal system into account are normally used to calculate temperature rise under these conditions.

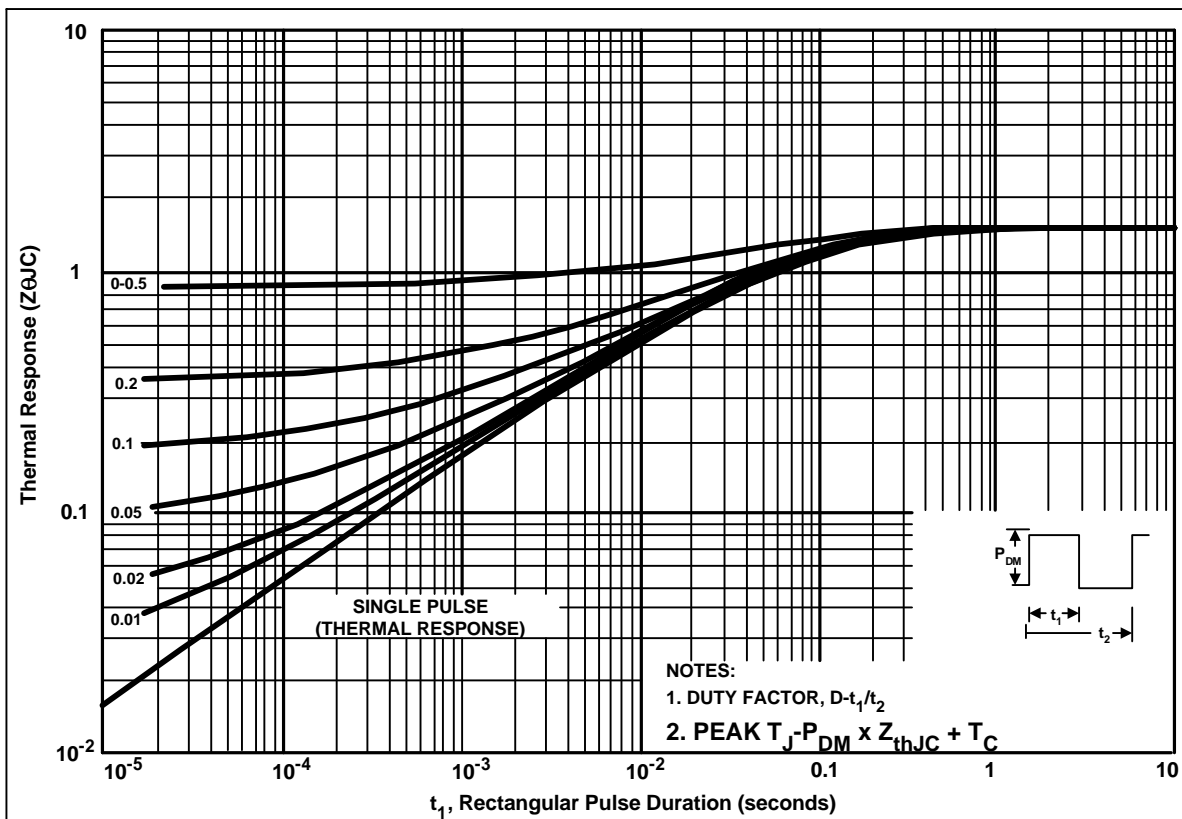


Figure 2. Transient Thermal Impedance Curves for IRF530 HEXFET

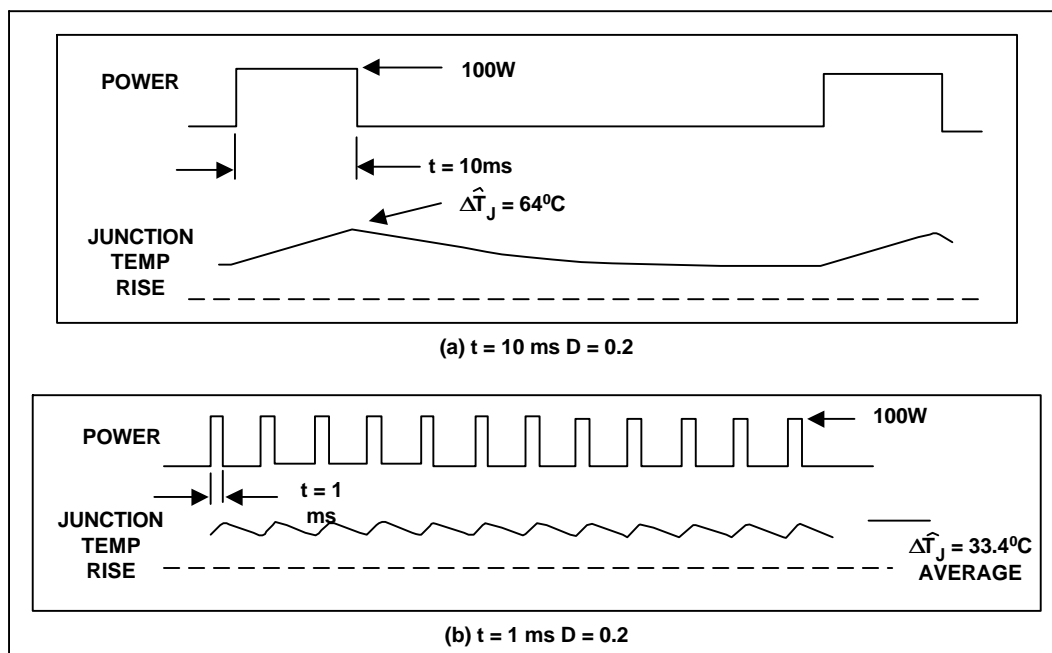


Figure 3. Waveforms of Power and Junction Temperature for Repetitive Operation, showing that Peak Junction Temperature is function of Operating Frequency. IRF330

6. PEAK CURRENT RATINGS

IGBTs and MOSFETs are able to carry peak current well in excess of their continuous current rating, provided that the rated junction temperature is not exceeded. There is, however, an upper limit on the permissible current, defined by the rated peak current. Most devices have a peak rating, that is several times their continuous rating at $T_c = 25^\circ\text{C}$.

Power transistors are fundamentally “linear” devices, as opposed to “latching” devices. As current increases, the point eventually is reached at which they go into “linear” operation and start to act, in effect, as a current limiter. This point depends upon the drive voltage applied to the gate, the safe limit of which is determined by the thickness of the oxide that insulates the gate from the body of the device. Peak ratings of power devices are normally achievable with an applied gate voltage that is equal to the maximum permissible gate voltage of 20V. They are repetitive ratings, as long as the junction temperature is kept within the rated T_{Jmax} . Peak junction temperature can be calculated from the thermal impedance data for the device, as indicated above.

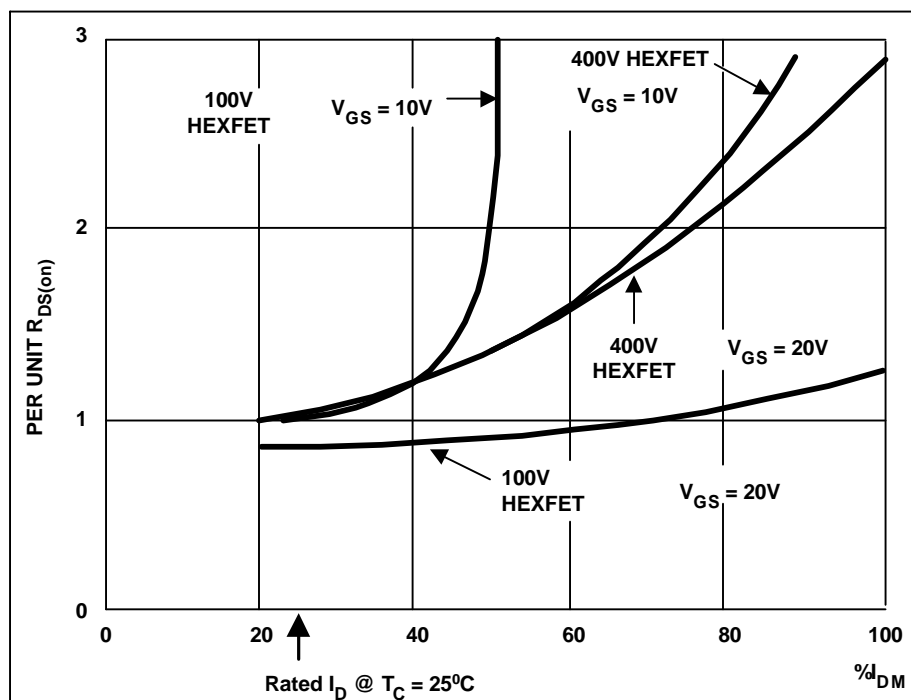


Figure 4. Typical Variation of On-Resistance with Drain Current.

It should be pointed out that the on-resistance of any MOSFET does increase as current increases. As shown in Figure 4, the on-resistance of a 100V rated HEXFET[®] at its rated I_{DM} with 20V applied to the gate is typically 1.4 x the value at the rated I_D ; the corresponding multiplier for a 400V rated HEXFET[®] is 2.9. This increase of on-resistance must, of course, be taken into account when making thermal calculations and designing for use of the I_{DM} rating.

APPENDIX

Determining the RMS Value of I_D Waveforms

To accurately determine the conduction losses in a MOSFET, the RMS value for I_D must be known. The current waveforms are rarely simple sinusoids or rectangles, and this can pose some problems in determining the value for I_{RMS} . The following equations and procedure can be used to determine I_{RMS} for any waveform that can be broken up into segments for which the RMS value can be calculated individually.

$$\text{The RMS value of any waveform is defined as } I_{RMS} = \sqrt{\frac{\int_0^t I^2(t)dt}{T}} \quad (1)$$

Figure A-1 shows several simple waveforms and the derivation for I_{RMS} using equation (1).

If the actual waveform can be approximated satisfactorily by combining the waveforms in Figure A-1, then the RMS value of the waveform can be calculated from: $I_{RMS} = \sqrt{I_{RMS(1)}^2 + I_{RMS(2)}^2 + \dots + I_{RMS(N)}^2}$ (2)

This is true to the extent that no two waveforms are different from zero at the same time.

In some applications such as switching regulators, it is possible for the designer to control the wave shape with topology or magnetic design. This can be very beneficial in reducing the value for I_{RMS} in the switch for a given value of average current.

EFFECT OF WAVEFORM SHAPE ON RMS VALUE

In a switch mode converter, the current waveforms through the inductors, transformer windings rectifiers and switches will appear as shown in Figure A-1, ranging from a triangle to a rectangle depending on the value of the averaging inductor and load.

The RMS content of the current waveform changes accordingly and this has a bearing on the MOSFET conduction losses that are proportional to I_{RMS}^2 .

A measure of the squareness of the waveform can be obtained from the ratio: $K = \frac{I_a}{I_b}$

It can be shown that: $K = \frac{I_a}{I_b} = f(L, L_c)$ where:

- L = inductance of the averaging choke.
- L_c = l is the critical inductance for a particular input voltage and load power.

As L is increased, K goes from 0 (triangle) to 1 (rectangle).

From the above expression and $I_{avg} = \frac{I_a + I_b}{2}$

we have: $I_a = \frac{2K}{K+1} I_{avg}$,

$$I_b = \frac{2}{K+1} I_{avg}$$

Substituting into the RMS expression for a trapezoidal waveform, shown in Figure A-1, we have:

$$I_{RMS} = 2\sqrt{D} I_{avg} \sqrt{\frac{1+K+K^2}{3(K+1)^2}}$$

For constant $I_{(avg)}$ and D, the normalized ($I_{RMS} = 1$ for $K = 1$) I_{RMS} is as shown in Figure A-3. This curve shows that, for triangular current waveforms, the I^2R losses are 32% higher than for rectangular waveforms. It is also apparent that for $I_a / I_b > 0.6$, the improvement incurred by increasing L is only 2%, so from a practical point of view, L need only be about twice L_c .

Increasing the value of I_a / I_b increases the switch turn-on losses but decreases the turn-off losses. Since the turn-off losses tend to be larger than the turn-on losses, increasing I_a / I_b reduces the total switching loss also.

For the case of discontinuous inductor current ($L < L_c$), $I_a / I_b = 0$ and is no longer relevant, since the waveforms are now triangles.

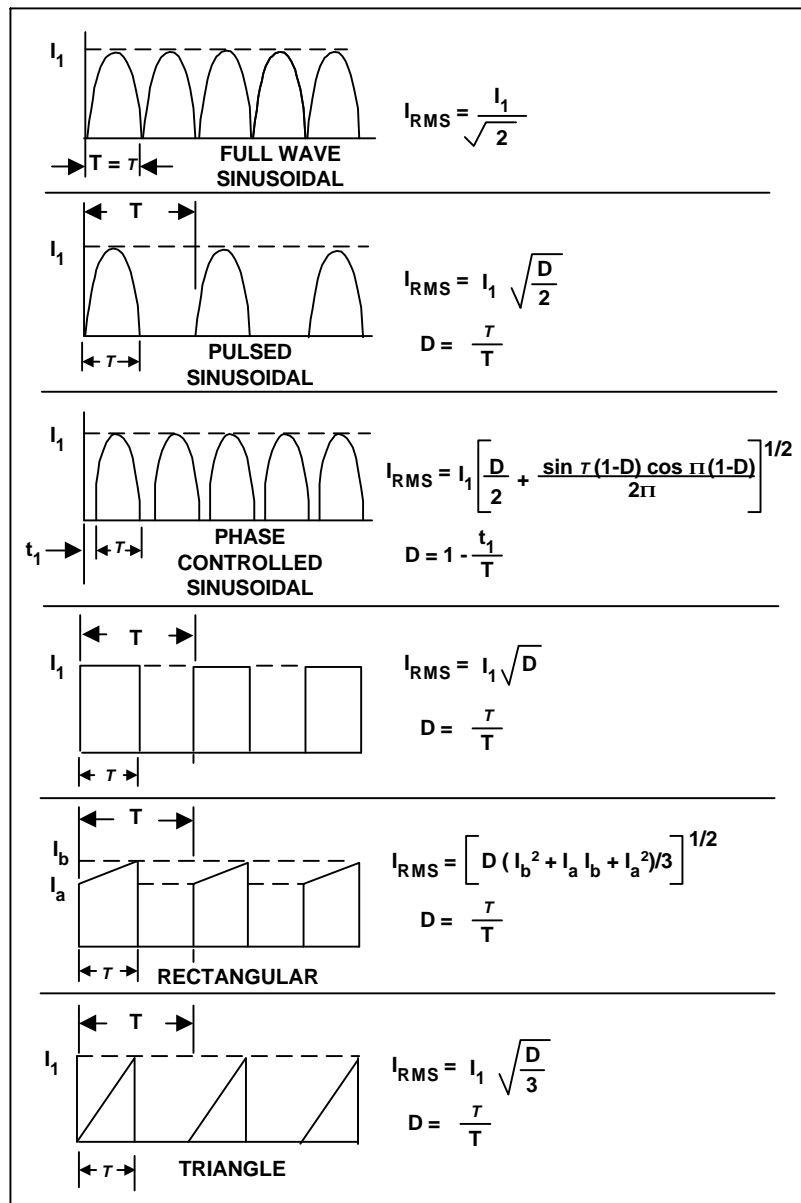


Figure A-1

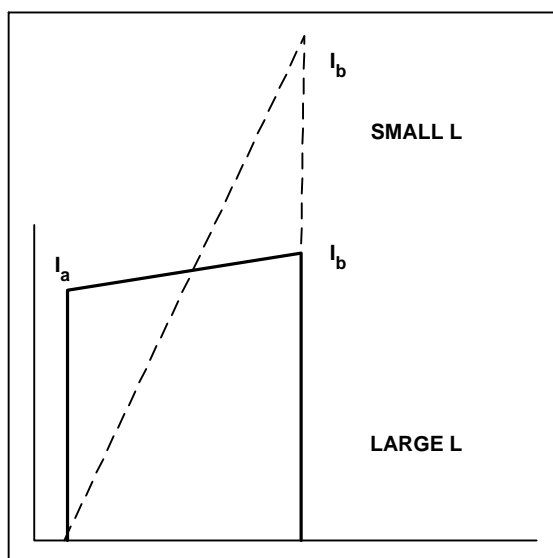


Figure A-2. Current Waveform

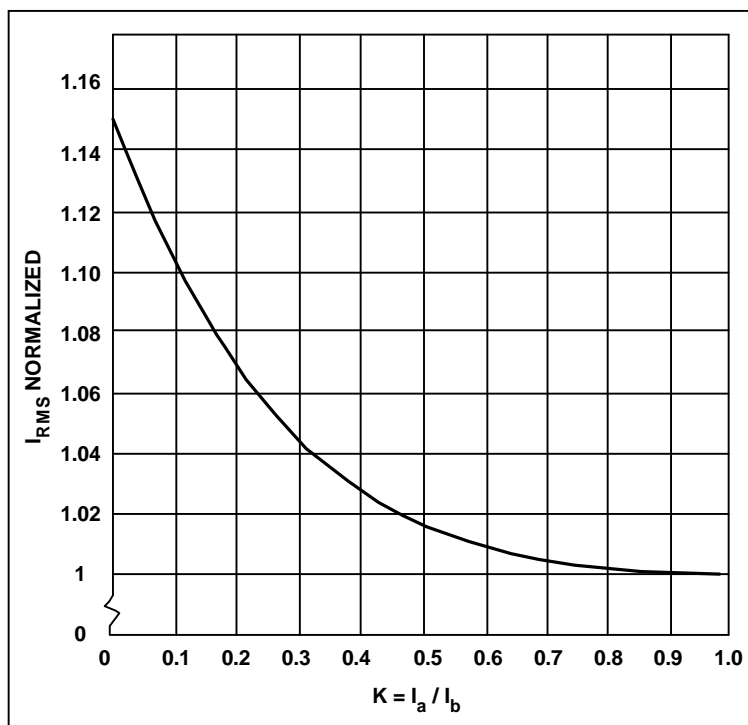


Figure A-3. Variation of IRMS with Squareness Ratio

Gate Drive Characteristics and Requirements for HEXFET[®]s

Topics covered:

- Gate drive vs base drive*
- Enhancement vs Depletion*
- N vs P-Channel*
- Max gate voltage*
- Zener diodes on gate?*
- The most important factor in gate drive: the impedance of the gate drive circuit*
- Switching 101 or Understanding the waveforms*
- What happens if gate drive impedance is high? dv/dt induced turn-on*
- Can a TTL gate drive a standard HEXFET[®]?*
- The universal buffer*
- Power dissipation of the gate drive circuit is seldom a problem*
- Can a C-MOS gate drive a standard HEXFET[®]?*
- Driving HEXFET[®]s from linear circuits*
- Drive circuits not referenced to ground*
- Gate drivers with optocouplers*
- Gate drive supply developed from the drain of the power device*
- Gate drivers with pulse transformers*
- Gate drivers with choppers*
- Drive requirements of Logic Level HEXFET[®]s*
- How fast is a Logic Level HEXFET[®] driven by a logic circuit?*
- Simple and inexpensive isolated gate drive supplies*
- A well-kept secret: Photovoltaic generators as gate drivers*
- Driving in the MHz? Use resonant gate drivers*
- Related topics*

(Note: Most of the gate drive considerations and circuits are equally applicable to IGBTs. Only MOSFETs are mentioned for the sake of simplicity. Special considerations for IGBTs are contained in INT-990)

1. GATE DRIVE VS BASE DRIVE

The conventional bipolar transistor is a current-driven device. As illustrated in Figure 1(a), a current must be applied between the base and emitter terminals to produce a flow of current in the collector. The amount of a drive required to produce a given output depends upon the gain, but invariably a current must be made to flow into the base terminal to produce a flow of current in the collector.

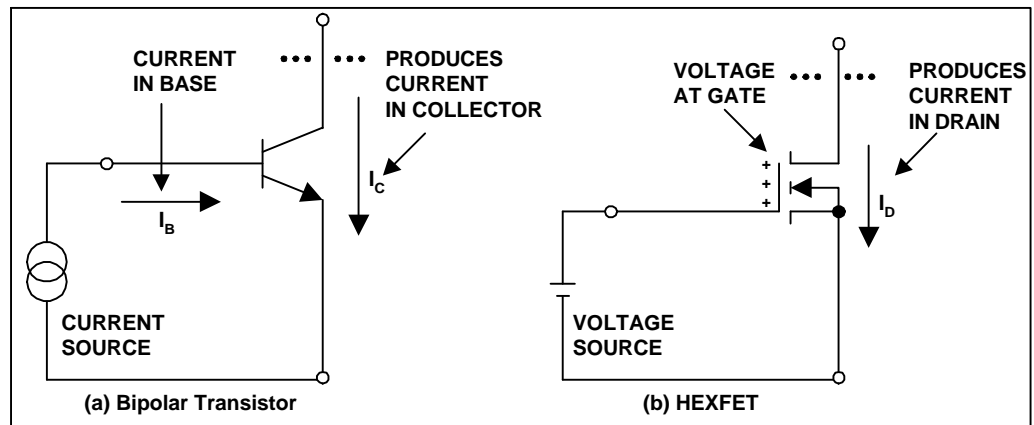


Figure 1. Bipolar Transistor is Current Driven, HEXFET is Voltage Driven

The HEXFET[®] is fundamentally different: it is a voltage-controlled power MOSFET device. A voltage must be applied between the gate and source terminals to produce a flow of current in the drain (see Figure 1b). The gate is isolated electrically from the source by a layer of silicon dioxide. Theoretically, therefore, no current flows into the gate when a DC voltage is applied to it - though in practice there will be an extremely small current, in the order of nanoamperes. With no voltage applied between the gate and source electrodes, the impedance between the drain and source terminals is very high, and only the leakage current flows in the drain.

When a voltage is applied between the gate and source terminals, an electric field is set up within the HEXFET[®]. This field “inverts” the channel (Figure 2) from P to N, so that a current can flow from drain to source in an uninterrupted sequence of N-type silicon (drain-channel-source). Field-effect transistors can be of two types: enhancement mode and depletion mode. Enhancement-mode devices need a gate voltage of the same sign as the drain voltage in order to pass current.

Depletion-mode devices are naturally on and are turned off by a gate voltage of the same polarity as the drain voltage. All HEXFET[®]s are enhancement-mode devices.

All MOSFET voltages are referenced to the source terminal. An N-Channel device, like an NPN transistor, has a drain voltage that is positive with respect to the source. Being enhancement-mode devices, they will be turned on by a positive voltage on the gate. The opposite is true for P-Channel devices, that are similar to PNP transistors.

Although it is common knowledge that HEXFET[®] transistors are more easily driven than bipolars, a few basic considerations have to be kept in mind in order to avoid a loss in performance or outright device failure.

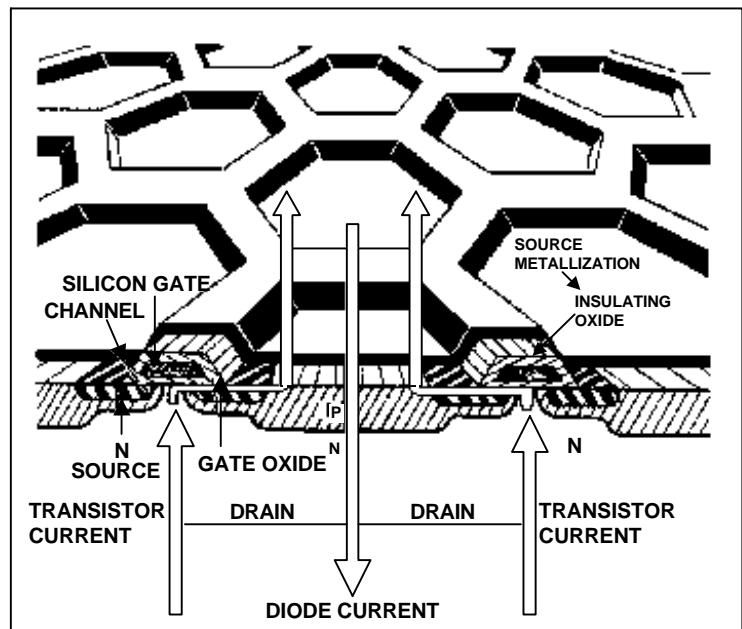


Figure 2. Basic HEXFET Structure

2. GATE VOLTAGE LIMITATIONS

Figure 2 shows the basic HEXFET[®] structure. The silicon oxide layer between the gate and the source regions can be punctured by exceeding its dielectric strength. The data sheet rating for the gate-to-source voltage is between 10 and 30 V for most HEXFET[®]s.

Care should be exercised not to exceed the gate-to-source maximum voltage rating. Even if the applied gate voltage is kept below the maximum rated gate voltage, the stray inductance of the gate connection, coupled with the gate capacitance, may generate ringing voltages that could lead to the destruction of the oxide layer. Overvoltages can also be coupled through the drain-gate self-capacitance due to transients in the drain circuit. A gate drive circuit with very low impedance insures that the gate voltage is not exceeded in normal operation. This is explained in more detail in the next section.

Zeners are frequently used “to protect the gate from transients”. Unfortunately they also contribute to oscillations and have been known to cause device failures. A transient can get to the gate from the drive side or from the drain side. In either case, it would be an indication of a more fundamental problem: a high impedance drive circuit. A zener would compound this problem, rather than solving it. Sometimes a zener is added to reduce the ringing generated by the leakage of a gate drive transformer, in combination with the input capacitance of the MOSFET. If this is necessary, it is advisable to insert a small series resistor (5-10 Ohms) between the zener and the gate, to prevent oscillations.

3. THE IMPEDANCE OF THE GATE CIRCUIT

To turn on a power MOSFET a certain charge has to be supplied to the gate to raise it to the desired voltage, whether in the linear region, or in the “saturation” (fully enhanced) region. The best way to achieve this is by means of a voltage source, capable of supplying any amount of current in the shortest possible time. If the device is operated as a switch, a large transient current capability of the drive circuit reduces the time spent in the linear region, thereby reducing the switching losses.

On the other hand, if the device is operated in the linear mode, a large current from the gate drive circuit minimizes the relevance of the Miller effect, improving the bandwidth of the stage and reducing the harmonic distortion. This can be better understood by analyzing the basic switching waveforms at turn-on and turn-off for a clamped inductive load, as shown in Figures

3 and 5. Figure 3 shows the waveforms of the drain current, drain-to-source voltage and gate voltage during the turn-on interval. For the sake of simplicity, the equivalent impedance of the drive circuit has been assumed as purely resistive.

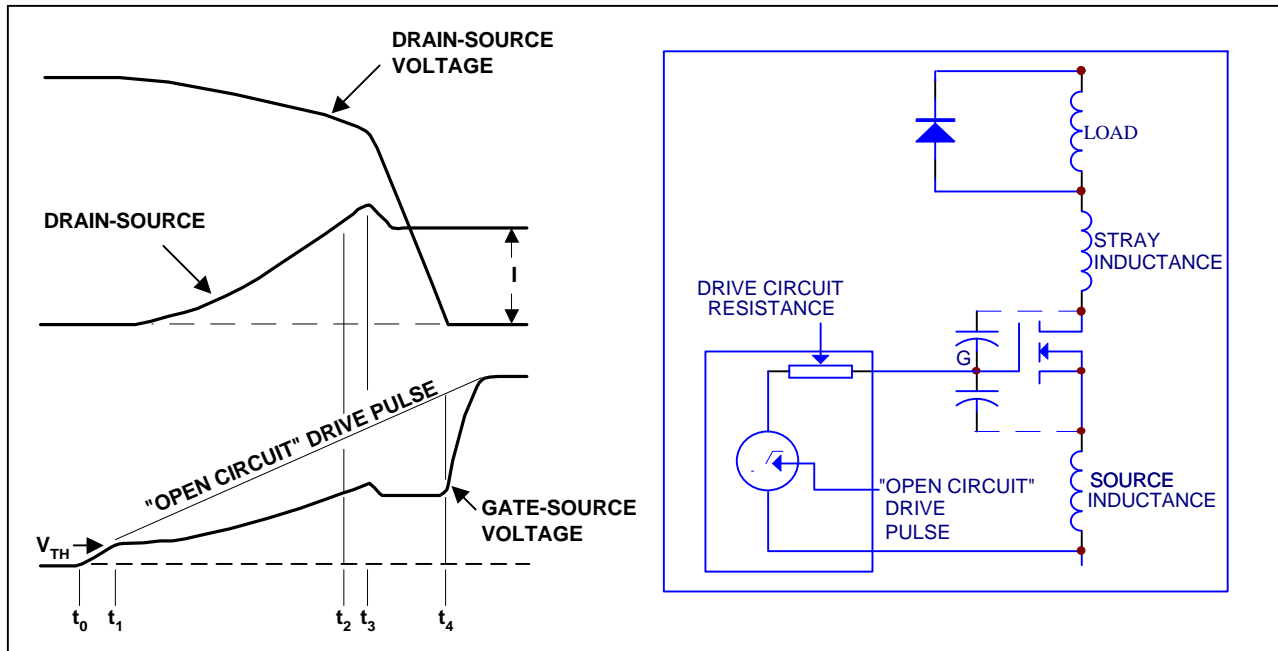


Figure 3. Waveforms at Turn-On

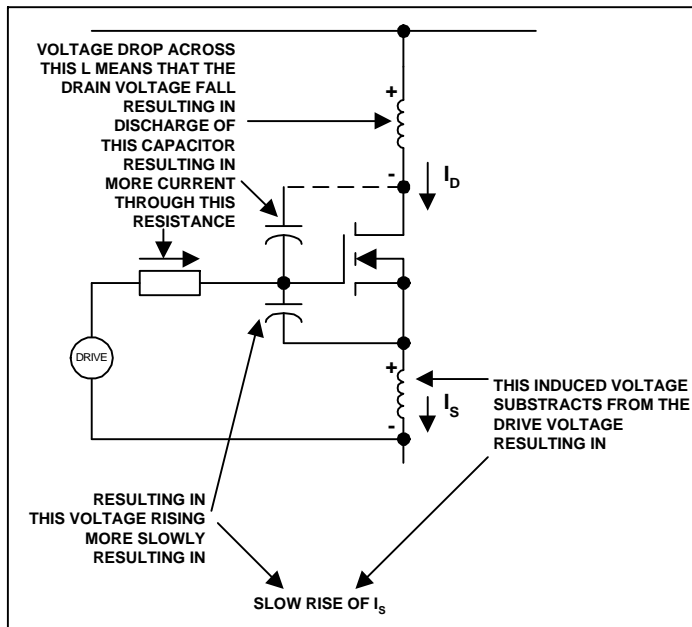


Figure 4. Diagrammatic Representation of Effects When Switching-ON

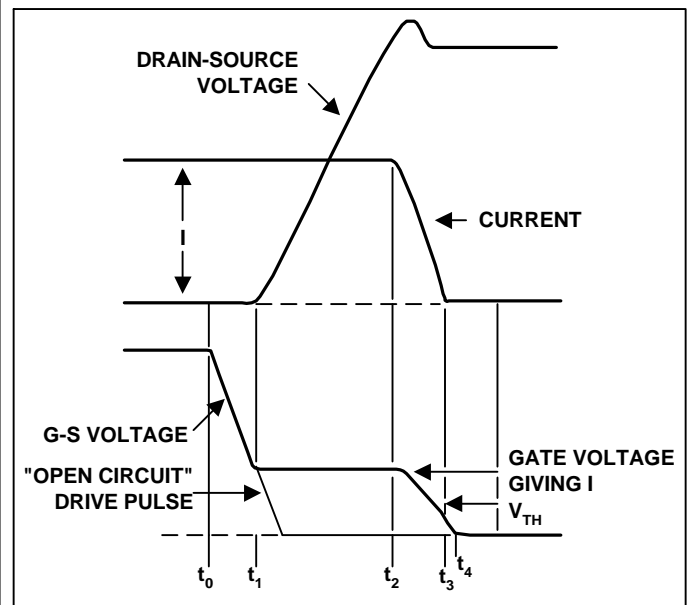


Figure 5. Waveforms at Turn-OFF

At time, t_0 , the drive pulse starts to rise. At t_0 it reaches the threshold voltage of the HEXFET[®]s and the drain current starts to increase. At this point, two things happen which make the gate-source voltage waveform deviate from its original “path”. First, inductance in series with the source which is common to the gate circuit (“common source inductance”) develops an induced voltage as a result of the increasing source current. This voltage counteracts the applied gate drive voltage, and slows down the rate of rise of voltage appearing directly across the gate and source terminals; this in turn slows down the rate of rise of the source current. This is a negative feedback effect: increasing current in the source produces a counteractive voltage at the gate, which tends to resist the change of current.

The second factor that influences the gate-source voltage is the so called “Miller” effect. During the period t_1 to t_2 some voltage is dropped across “unclamped” stray circuit inductance in series with the drain, and the drain-source voltage starts to fall. The

decreasing drain-source voltage is reflected across the drain-gate capacitance, pulling a discharge current through it, and increasing the effective capacitive load on the drive circuit.

This in turn increases the voltage drop across the source impedance of the drive circuit, and decreases the rate of rise of voltage appearing between the gate and source terminals. Obviously, the lower the impedance of the gate drive circuit, the less this effect will be. This also is a negative feedback effect; increasing current in the drain results in a fall of drain-to-source voltage, which in turn slows down the rise of gate-source voltage, and tends to resist the increase of drain current. These effects are illustrated diagrammatically in Figure 4. This state of affairs continues throughout the period t_1 to t_2 , as the current in the HEXFET[®] rises to the level of the current, I_M , already flowing in the freewheeling rectifier, and it continues into the next period, t_2 to t_3 , when the freewheeling rectifier goes into reverse recovery.

Finally, at time t_3 the freewheeling rectifier starts to support voltage and drain current and voltage start to fall. The rate of fall of drain voltage is now governed almost exclusively by the Miller effect, and an equilibrium condition is reached, under which the drain voltage falls at just the rate necessary for the voltage between gate and source terminals to satisfy the level of drain current established by the load. This is why the gate-to-source voltage falls as the recovery current of the freewheeling rectifier falls, then stays constant at a level corresponding to the drain current, while the drain voltage falls. Obviously, the lower the impedance of the gate-drive circuit, the higher the discharge current through the drain-gate self-capacitance, the faster will be the fall time of the drain voltage and the switching losses.

Finally, at time t_4 , the HEXFET[®] is switched fully on, and the gate-to-source voltage rises rapidly towards the applied "open circuit" value.

Similar considerations apply to the turn-off interval. Figure 5 shows theoretical waveforms for the HEXFET[®] in the circuit of Figure 4 during the turn-off interval. At t_0 the gate drive starts to fall until, at t_1 , the gate voltage reaches a level that just sustains the drain current and the device enters the linear mode of operation. The drain-to-source voltage now starts to rise. The Miller effect governs the rate-of-rise of drain voltage and holds the gate-to-source voltage at a level corresponding to the constant drain current. Once again, the lower the impedance of the drive circuit, the greater the charging current into the drain-gate capacitance, and the faster will be the rise time of the drain voltage. At t_3 the rise of drain voltage is complete, and the gate voltage and drain current start to fall at a rate determined by the gate-source circuit impedance.

We have seen how and why a low gate drive impedance is important to achieve high switching performance. However, even when switching performance is of no great concern, it is important to minimize the impedance in the gate drive circuit to clamp unwanted voltage transients on the gate. With reference to Figure 6, when one HEXFET[®] is turned on or off, a step of voltage is applied between drain and source of the other device on the same leg. This step of voltage is coupled to the gate through the gate-to-drain capacitance, and it can be large enough to turn the device on for a short instant ("dv/dt induced turn-on"). A low gate drive impedance would keep the voltage coupled to the gate below the threshold.

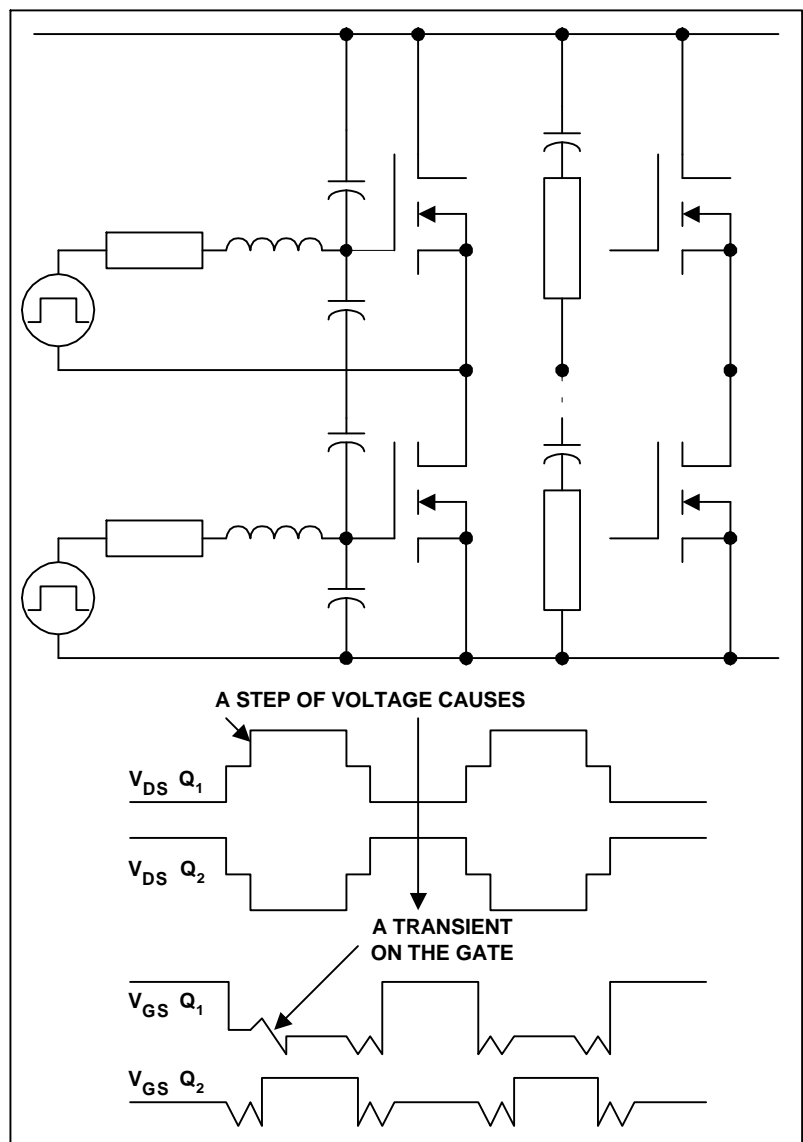


Figure 6. Transients of Voltage Induced on the Gate by Rapid Changes on the Drain-to-Source Voltage

In summary: MOS-gated transistors should be driven from low impedance (voltage) sources, not only to reduce switching losses, but to avoid dv/dt induced turn-on and reduce the susceptibility to noise.

4. DRIVING STANDARD HEXFET[®]S FROM TTL

Table 1 shows the guaranteed sourcing and sinking currents for different TTL families at their respective voltages. From this table, taking as an example of the 74LS series, it is apparent that, even with a sourcing current as low as 0.4 mA, the guaranteed logic one voltage is 2.4V (2.7 for 74LS and 74S). This is lower than the possible threshold of a HEXFET[®]. The use of a pull-up resistor in the output, as shown in Figure 7, takes the drive voltage up to 5 V, as necessary to drive the gate of Logic Level HEXFET[®]s, but is not sufficient to fully enhance standard HEXFET[®]s. Section 8 covers the drive characteristics of the logic level devices in detail.

Logic Conditions	54 / 74	54H / 74H	(54L) / 74L	(54LS) / 74LS	74S
Logic Zero Min. sink current for V_{OL}	16mA $\leq 0.4V$	20mA $\leq (0.4V) /$	20mA $\leq (0.3V) /$ 0.4V	(4) / 8 $\leq (0.4V) /$ 0.5V	20mA 0.5V
Logic One Max. source current for V_{OH}	-0.4mA $\geq 2.4V$	-0.5mA $\geq 2.4V$	-0.2mA $\geq 2.4V$	-0.4mA $\geq (2.5) /$ 2.7V	-1.0mA $\geq 2.7V$
Typical Gate Propagation Delay	10ns	7ns	50ns	12ns	4ns

Table 1. Driving HEXFET[®]s from TTL (Totem Pole Outputs)

Open collector buffers, like the 7406, 7407, etc., possibly with several drivers connected in parallel as shown in Figure 9, give enough voltage to drive standard devices into “full enhancement”, i.e. data sheet on-resistance. The impedance of this drive circuit, however, gives relative long switching times. Whenever better switching performance is required, interface circuits should be added to provide fast current sourcing and sinking to the gate capacitances. One simple interface circuit is the complementary source-follower stage shown in Figure 9. To drive a MOSFET with a gate charge of 60 nC in 60 ns an average gate current of 1 A has to be supplied by the gate drive circuit, as indicated in INT-944. The on-resistance of the gate drive MOSFETs has to be low enough to support the desired switching times.

With a gate charge of 60 nC and at a switching frequency is 100kHz, the power lost in the gate drive circuit is approximately:

$$P = V_{GS} \times Q_G \times f = 12 \times 60 \times 10^{-9} \times 100 \times 10^3 = 72\text{mW}$$

The driver devices must be capable of supplying 1A without significant voltage drop, but hardly any power is dissipated in them.

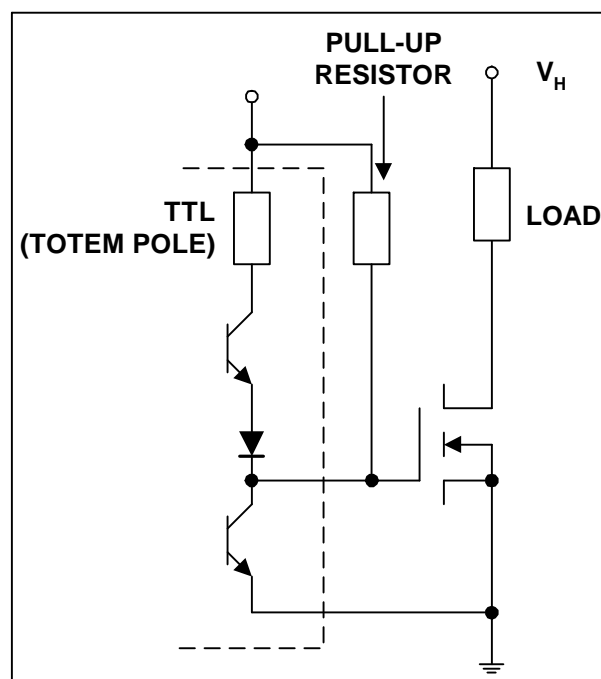


Figure 7. Direct Drive from TTL Output

5. DRIVING STANDARD HEXFET[®]S FROM C-MOS

While the same general considerations presented above for TTL would also apply to C-MOS, there are three substantial differences that should be kept in mind:

1. C-MOS has a more balanced source/sink characteristic that, on a first approximation, can be thought of as a 500 ohm resistance for operation over 8V and a 1k ohm for operation under 8V (Table 2).

2. C-MOS can operate from higher supply voltages than 5V so that HEXFET[®] saturation can be guaranteed.
3. Switching times are longer than those for TTL (Table 2).

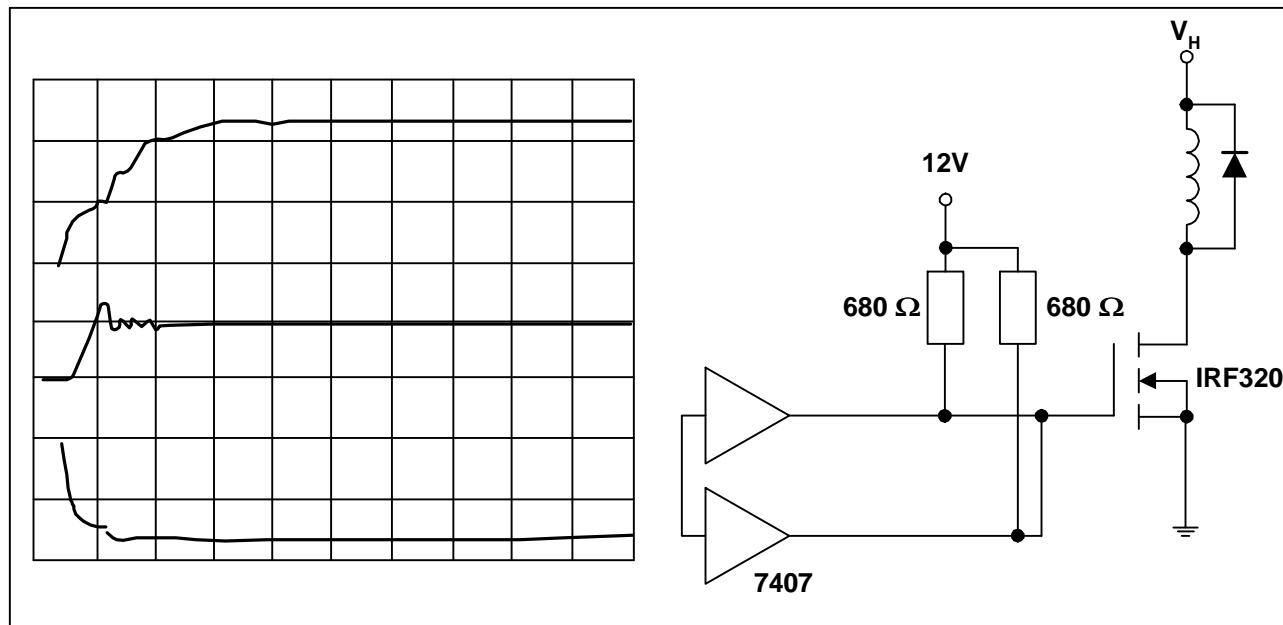


Figure 8. High Voltage TTL driver and its waveforms

When C-MOS outputs are directly coupled to the gate of a HEXFET[®], the dominant limitation to performance is not the switching time, but the internal impedance (assuming that C-MOS are operated from a 10V or higher voltage supply). It will certainly not be able to turn OFF the HEXFET[®] as fast as the TTL, while the turn-ON waveform will be slightly better than what can be achieved with a 7407 with a 680 ohm pull-up resistor. Of course, gates can be paralleled in any number to lower the impedance and this makes C-MOS a very simple and convenient means of driving HEXFET[®]s. Drivers can also be used, like the 4049 and 4050 which have a much higher current sinking capability (Table 2), but they do not yield any significant improvement in current sourcing.

For better switching speeds, buffer circuits, like the one shown in Figure 9, should be considered, not only to provide better current sourcing and sinking capability, but also to improve over the switching times of the C-MOS output itself and the dv/dt noise immunity.

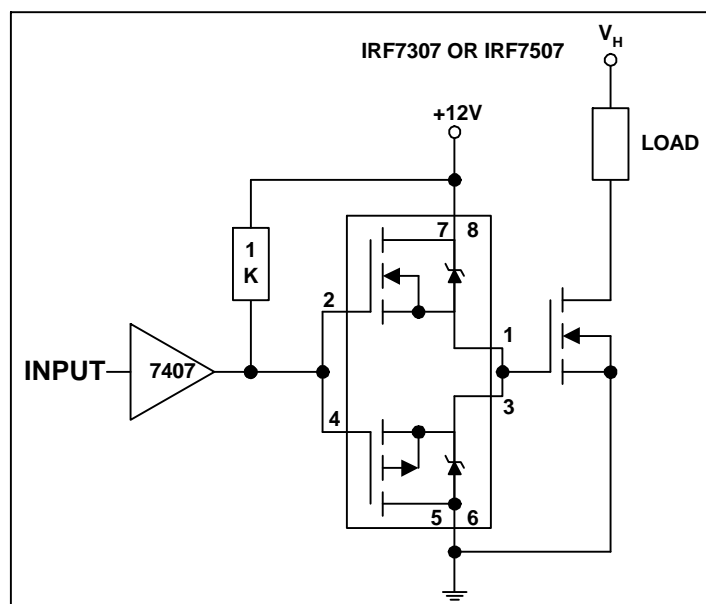


Figure 9. Simple Interface to Drive HEXFETs from TTL

6. DRIVING HEXFET[®]S FROM LINEAR CIRCUITS

The complementary source follower configuration of Figure 9 can also be used in linear applications to improve drive capability from an opamp or other analog source.

Most operational amplifiers have a very limited slew rate, in the order of few V/microsec. This would limit the bandwidth to less than 25kHz. A larger bandwidth can be obtained with better operational amplifiers followed by a current booster, like the ones shown in Figures 10 or 11. For a system bandwidth of 1MHz, the opamp bandwidth must be significantly higher than 1MHz and its slew rate at least 30V/ μ s.

Logic Supply Voltage Logic Conditions	Standard Buffered Outputs			4049 / 4050 Drivers		
	5V	10V	15V	5V	10V	15V
Logic Zero: Approximate sink current for $V_{OL} \leq 1.5V$	1.5mA	3.5mA	4mA	20mA	40mA	40mA
Logic One: Minimum source current for V_{OH}	-0.5mA $\geq 4.6V$	-13mA $\geq 9.5V$	-3.4mA $\geq 13.5V$	-1.25mA $\geq 2.5V$	-1.25mA $\geq 9.5V$	-3.75mA $\geq 13.5V$
Typical switching times of logic drive signals:						
RISE	100ns	50ns	40ns	100ns	50ns	40ns
FALL	100ns	50ns	40ns	40ns	20ns	15ns

Table 2. Driving HEXFET[®]s from C-MOS (Buffered)

When analog signals determine the switching frequency or duty cycle of a HEXFET[®], as in PWM applications, a voltage comparator is normally used to command the switching. Here, too, the limiting factors are the slew rate of the comparator and its current drive capability. Response times under 40ns can be obtained at the price of low output voltage swing (TTL compatible). Once again, the use of output buffers like the ones shown in Figures 9, may be necessary to improve drive capability and dv/dt immunity. If better switching speeds are desired, a fast op-amp should be used.

In many applications, when the HEXFET[®] is turned on, current transfers from a freewheeling diode into the HEXFET[®]. If the switching speed is high and the stray inductances in the diode path are small, this transfer can occur in such a short time as to cause a reverse recovery current in the diode high enough to short out the dc bus. For this reason, it may be necessary to slow down the turn-on of the HEXFET[®] while leaving the turn-off as fast as practical. Low impedance pulse shaping circuits can be used for this purpose, like the ones in Figures 12 and 13.

7. DRIVE CIRCUITS NOT REFERENCED TO GROUND

To drive a HEXFET[®] into saturation, an appropriate voltage must be applied between the gate and source. If the load is connected between source and ground, and the drive voltage is applied between gate and ground, the effective voltage between gate and source decreases as the device turns on. An equilibrium point is reached in which the amount of current flowing in the load is such that the voltage between gate and source maintains that amount of drain current and no more. Under these conditions the voltage drop across the MOSFET is certainly higher than the threshold voltage and the power dissipation can be very high. For this reason, the gate drive circuit is normally referenced to the source rather than to the ground. There are

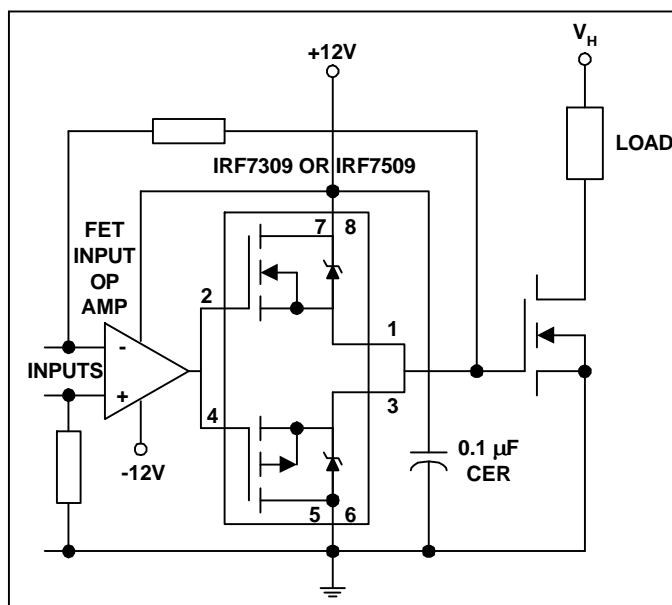


Figure 10. Dual Supply Op-Amp Drive Circuit

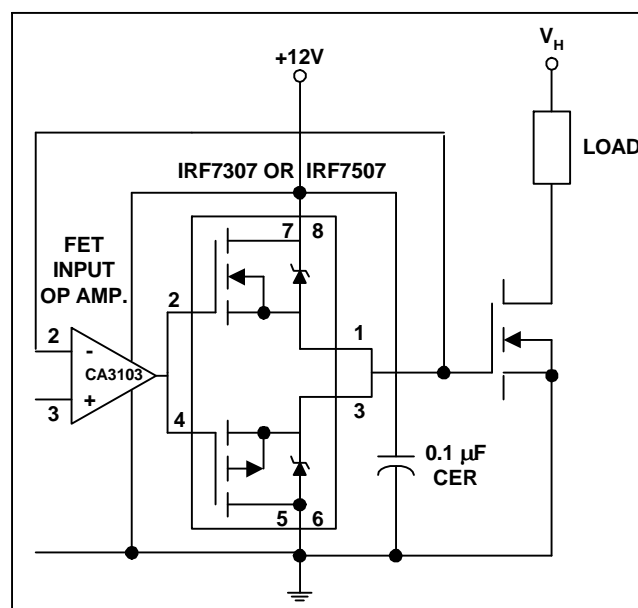


Figure 11. Single Supply Op-Amp Drive Circuit (Voltage Follower)

basically three ways of developing a gate drive signal that is referenced to a floating point:

1. By means of optically coupled isolators.
2. By means of pulse transformers.

By means of DC to DC chopper circuits with transformer isolation.

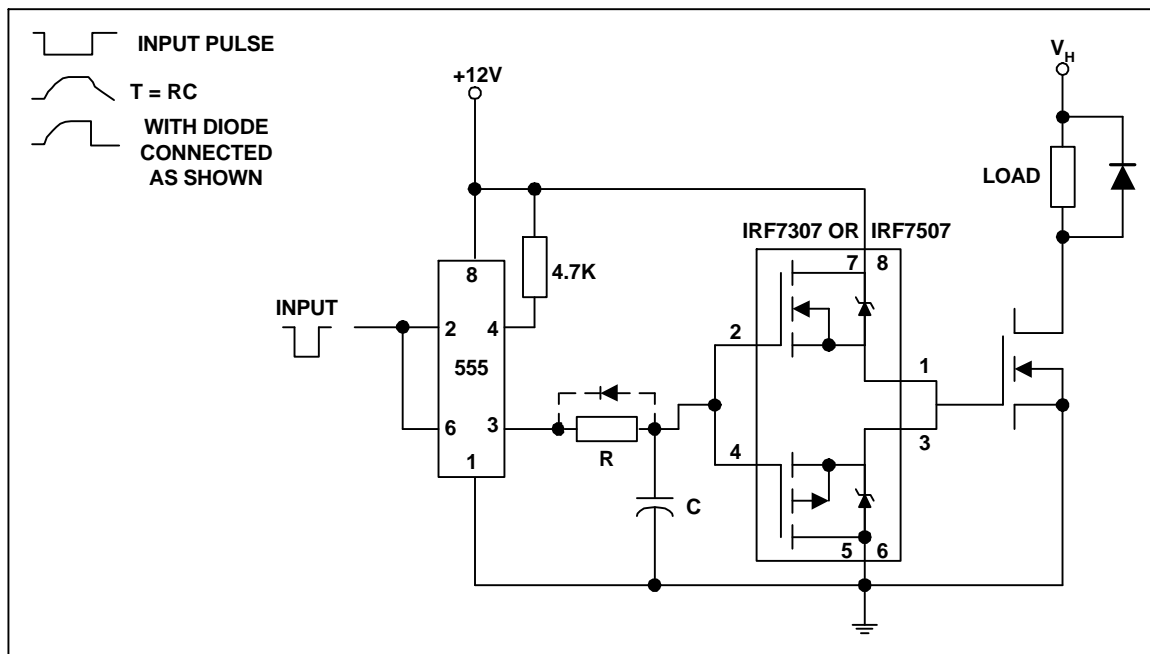


Figure 12. A pulse shaper. The 555 is used as an illustration of a Schmitt Trigger pulse shaper

7.1 MGDs with optocouplers

Most optocouplers require a separate supply grounded to the source on the receiving end of the optical link and a booster stage at the output, as shown in Figure 14a. One of the major difficulties encountered in the use of optocouplers is their susceptibility to noise. This is of particular relevance in applications where high currents are being switched rapidly. Because of the dv/dt seen by the V_{EE} pin, the optocoupler needs to be rated for high dv/dt , in the order of 10 V/ns.

Figure 15a shows an MGD with under-voltage lockout and negative gate bias. When powered with a 19 V floating source, the gate drive voltage swings between +15V and -3.9V. D1 and R2 offset the emitter voltage by 3.9V. The switching waveforms shown in Figure 15b are similar to those in Figure 14b except for the negative bias. Q3, D2 and R5 form the under voltage lockout circuit.

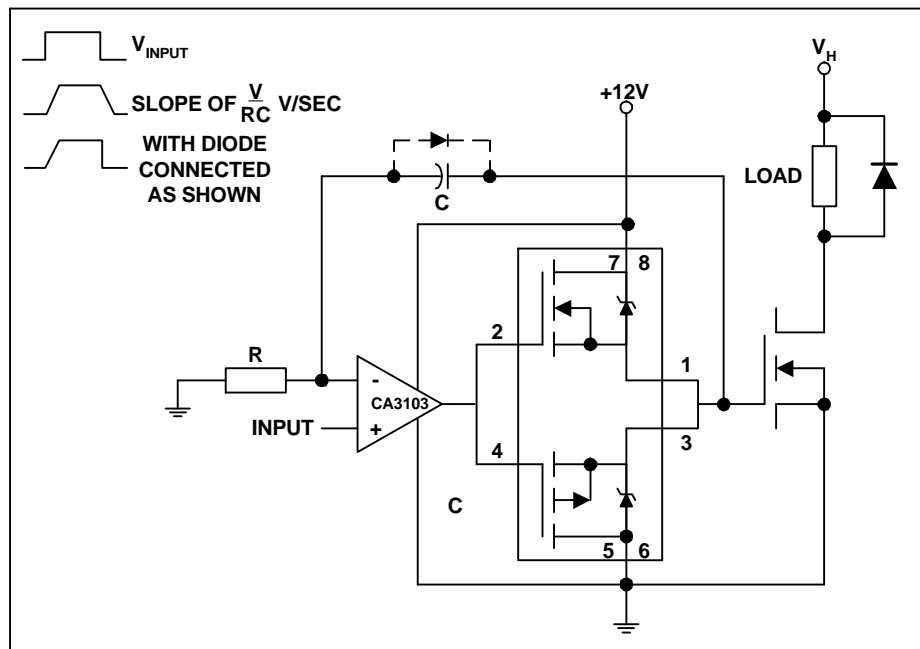


Figure 13. Pulse shaper implemented with an integrator

The LED D2 is used as low voltage, low current reference diode. Q3 turns on when the voltage at the anode of D2 exceeds the sum of the forward voltage of LED and the base-emitter voltage of Q3. This enables the operation of the optocoupler. The tripping point of the under voltage lock-out circuit is 17.5V. The start-up wave forms are shown in Figure 16.

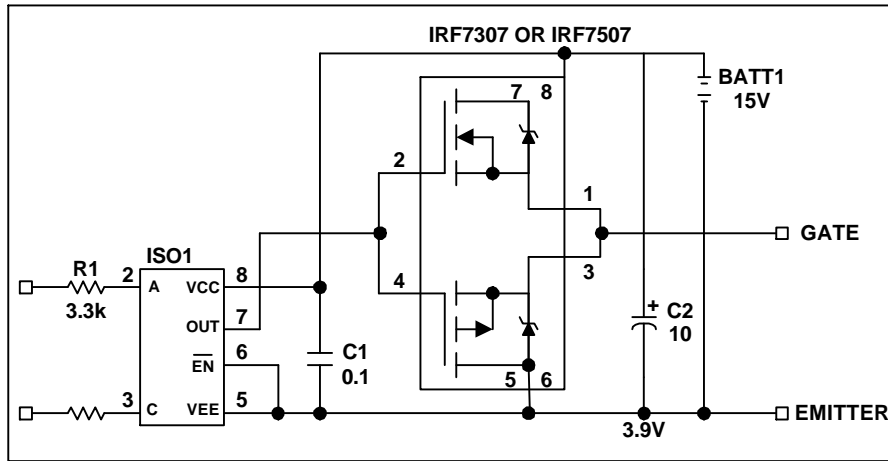


Figure 14a. Simple high current optoisolated driver

The auxiliary supply for the optocoupler and its associated circuitry can be developed from the drain voltage of the MOSFET itself, as shown in Figure 17, 18 and 19. This supply can be used in conjunction with the UV-lockout shown in Figure 15 to provide a simple high-quality optoisolated drive.

The circuit in Figure 17a can be modified to provide higher output current. By changing C1 to 680pF and R3 to 5.6k, its performance changes to what is shown in Figures 20, 21 and 22. Other methods of developing isolated supplies are discussed in Section 9.

7.2 Pulse transformers

A pulse transformer is, in principle, a simple, reliable and highly noise-immune method of providing isolated gate drive. Unfortunately it has many limitations that must be overcome with additional components. A transformer can only transfer to the secondary the AC component of the input signal. Consequently, their output voltage swings from negative to positive by an amount that changes with the duty cycle, as shown in Figure 23. As a stand-alone component they can be used for duty cycles between 35 and 65%.

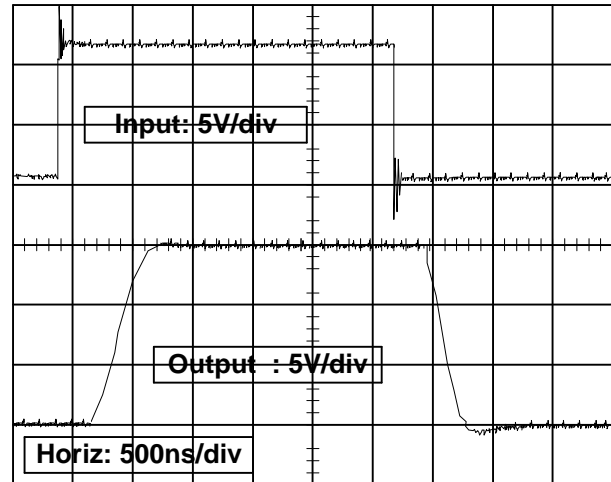


Figure 14b: Waveforms associated with the circuit of Figure 14a when loaded with 100nF

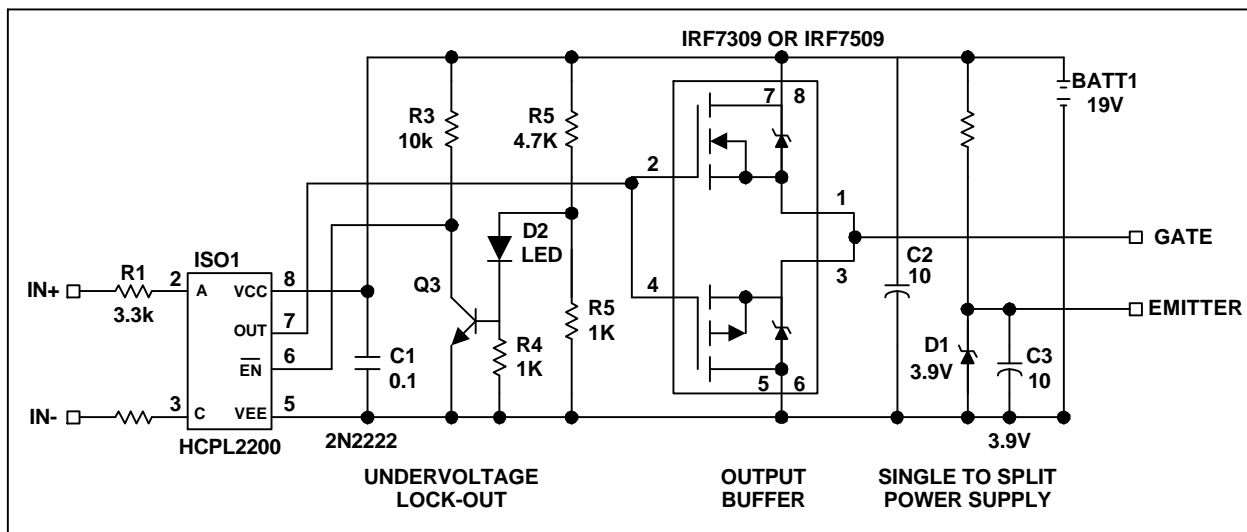


Figure 15a: Optoisolated driver with UV lockout and negative gate bias

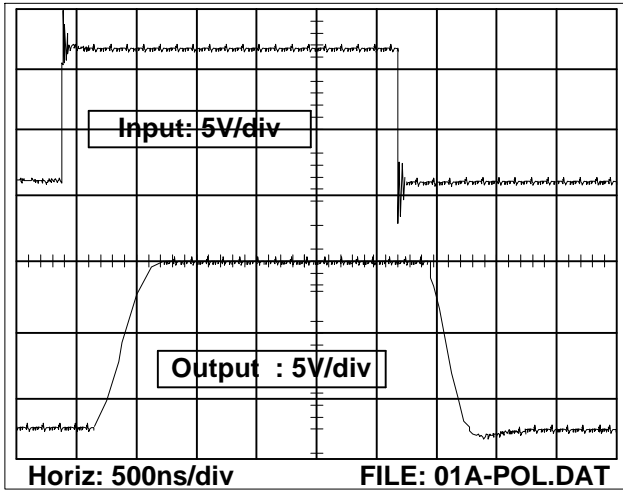


Figure 15b: Waveforms of the circuit in Figure 21a when loaded with 100nF

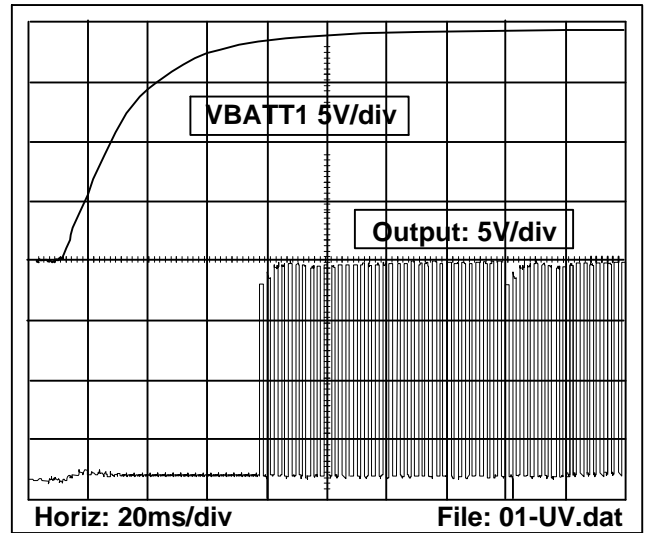


Figure 16. Start-up waveforms for the circuit of Figure 15a.

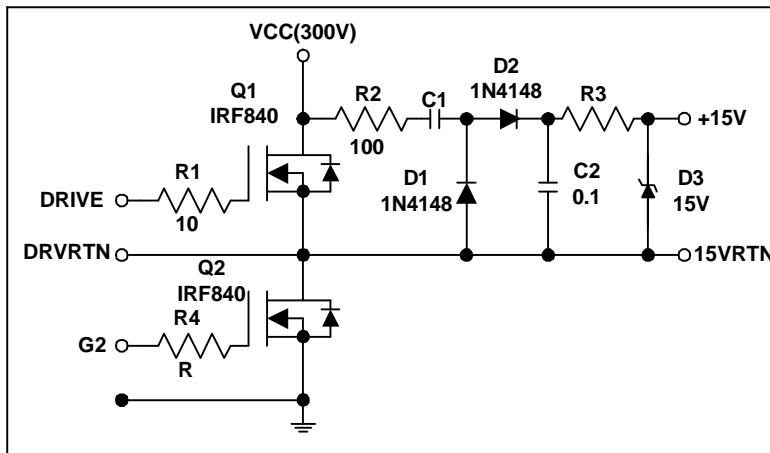


Figure 17a. Drive supply developed from the drain voltage

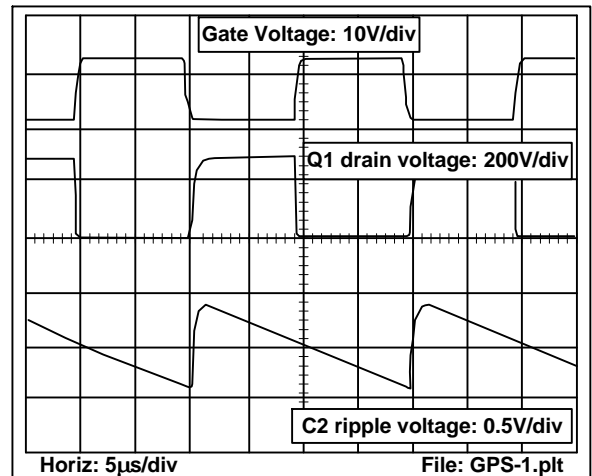


Figure 17b. Waveforms of the circuit in Figure 23a. C1 = 100 pF, R3 = 5.6 k, f = 50 kHz

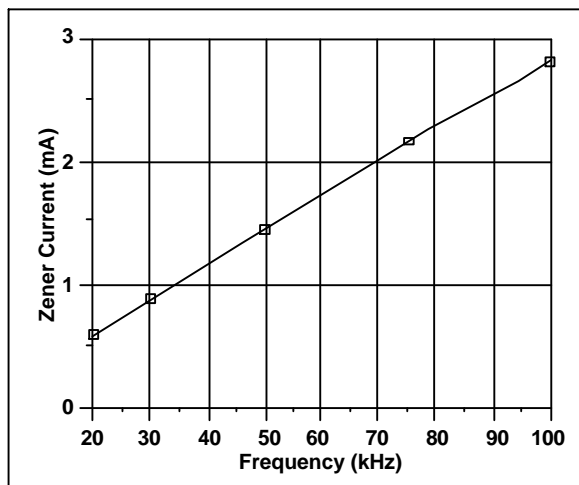


Figure 18. Zener current (max output current) for the circuit in Figure 23a.

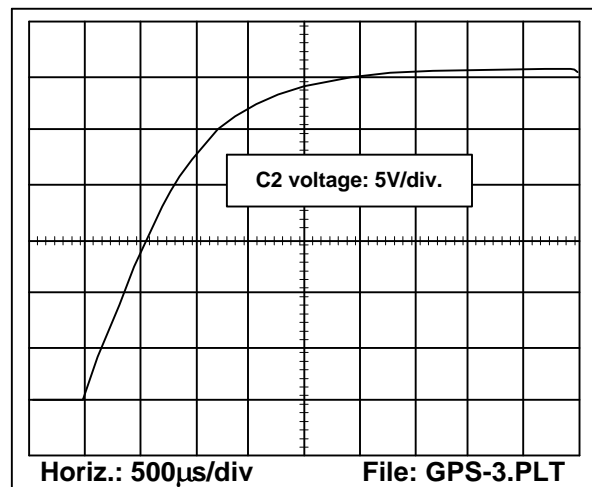


Figure 19. Start-up voltage at 50 kHz for the circuit in Figure 23a.

They have the additional advantage of providing a negative gate bias. One additional limitation of pulse transformers is the fact that the gate drive impedance is seriously degraded by the leakage inductance of the transformer. Best results are normally obtained with a few turns of twisted AWG30 wire-wrap wire on a small ferrite core.

Lower gate drive impedance and a wider duty-cycle range can be obtained with the circuit in Figure 24a. In this circuit, Q1 and Q2 (a single Micro-8 package) are used to buffer the input and drive the primary of the transformer. The complementary MOS output stage insures low output impedance and performs wave shaping. The output stage is fed by a dc restorer made by C2 and D1 that references the signal to the positive rail. D1 and D2 are also used to generate the gate drive voltage.

The input and output wave form with 1nF load capacitance are shown in Figure 24b. The turn-on and turn-off delays are 50ns. The rise and fall times are determined by the 10 Ohm resistor and the capacitive load. This circuit will operate reliably between 20 and 500 kHz, with on/off times from 0.5 to 15 microseconds.

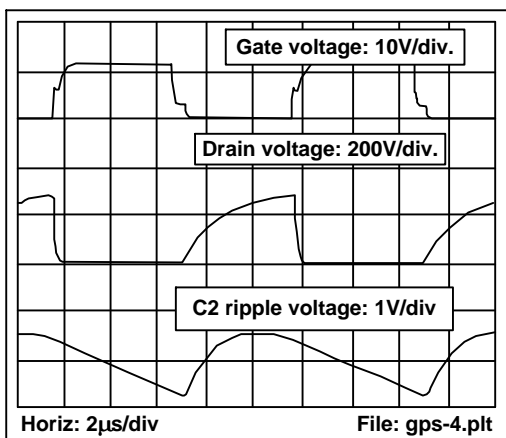


Figure 20. Waveforms of the circuit in Figure 23a. with $C1=680\text{pF}$, $R3=1\text{k}$, $f=100\text{kHz}$.

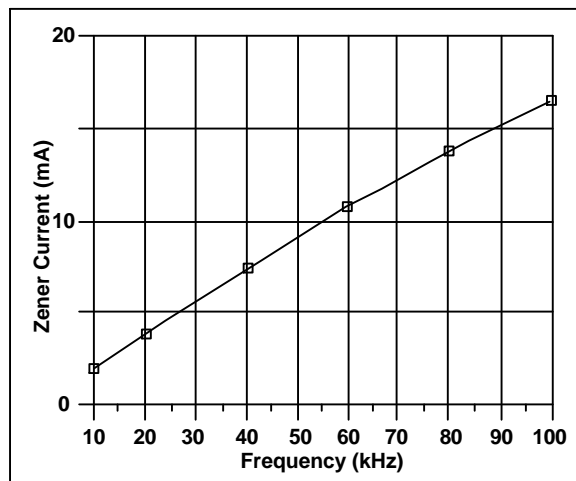


Figure 21. Zener current (max output current) for the circuit in Figure 23a. with $C1 = 680\text{pF}$, $R3 = 1\text{k}$

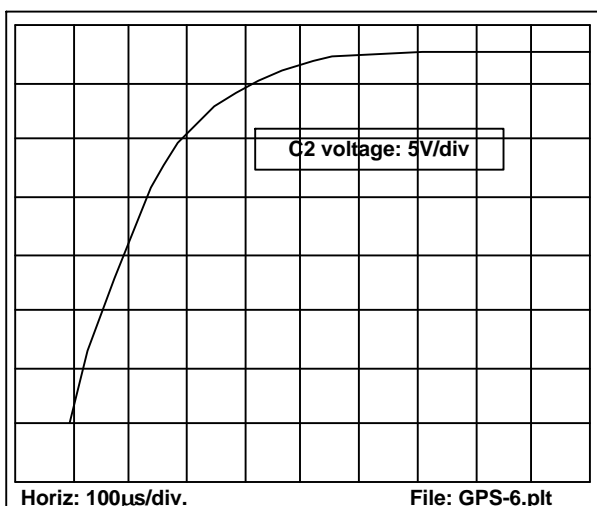


Figure 22. Start-up voltage at 100 kHz for the circuit in Figure 23a. with $C1=680\text{pF}$, $R3=R3=1\text{k}$

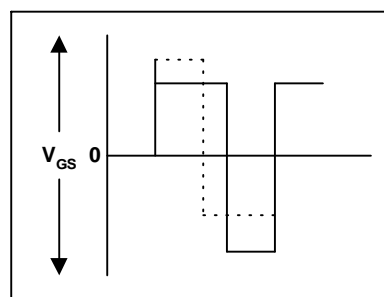


Figure 23. Volt-seconds across winding must balance

Due to the lack of an under voltage lock-out feature, the power-up and power down behavior of the circuit is important. Intentionally $C1$ and $C2$ are much bigger in value than $C3$ so that the voltage across $C3$ rises to an adequate level during the first incoming pulse. The power-up wave forms at 50kHz switching frequency and 50% duty cycle are shown in Figure 25. During the first pulse, the output voltage is 10V only, and drops back below 10V at the fifth pulse.

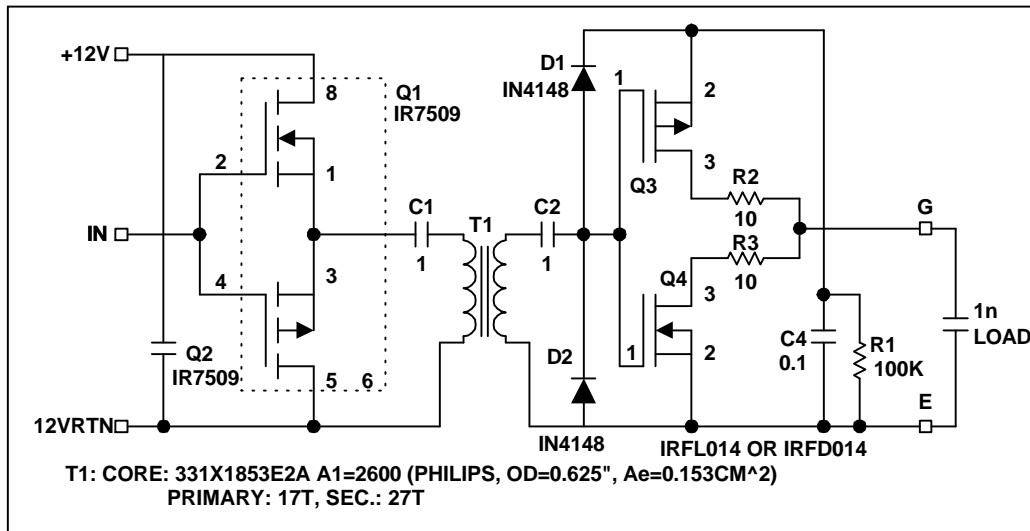


Figure 24a. Improving the performance of a gate drive transformer

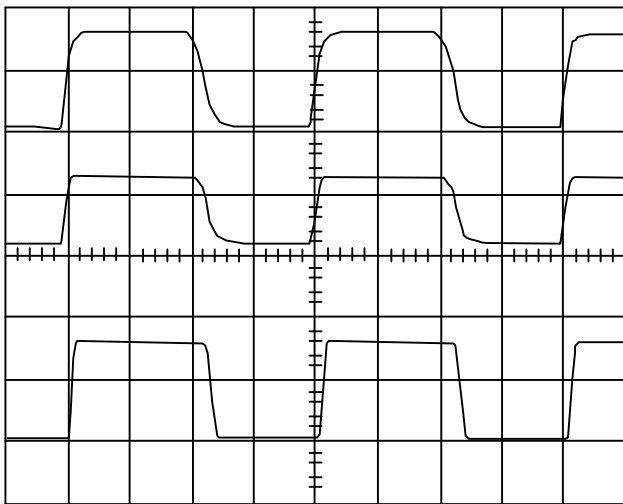


Figure 24b. Waveforms associated with the circuit of Figure 24a

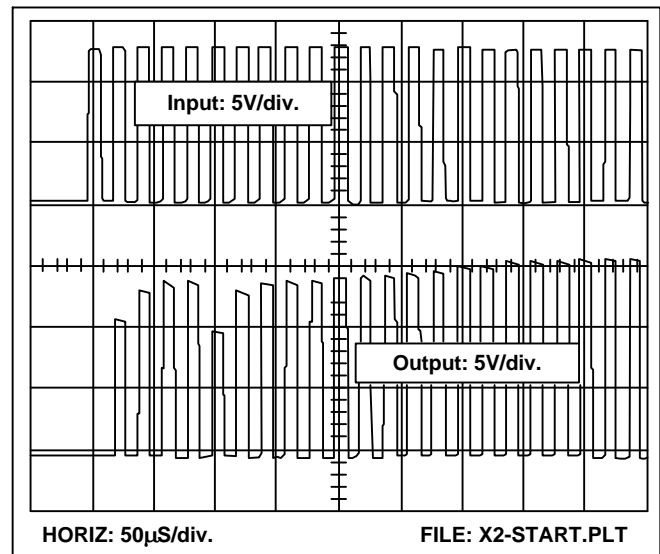


Figure 25. Waveforms during start-up for the circuit in Figure 24a.

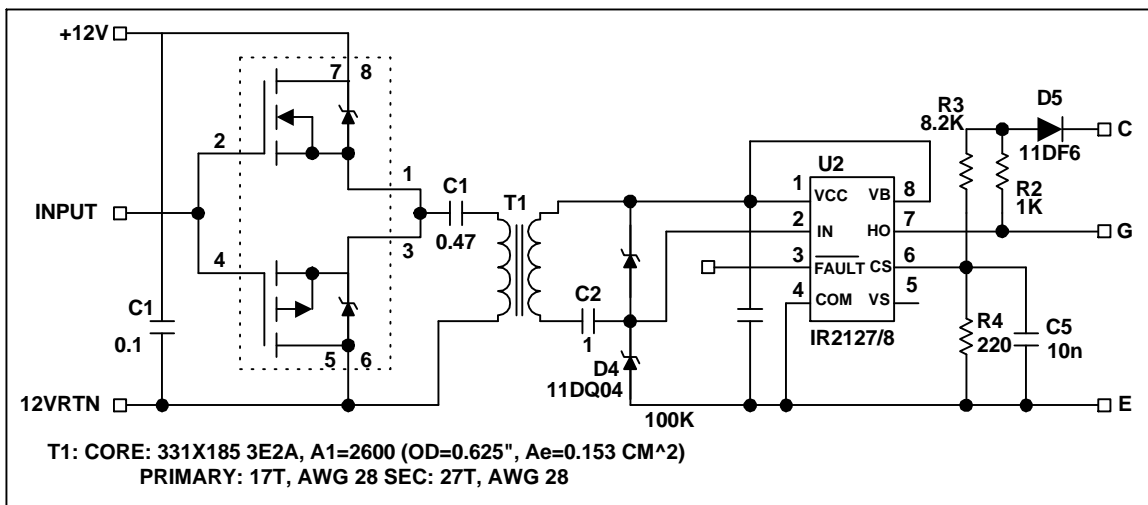


Figure 26a. Transformer-coupled MGD with UV lockout and short-circuit protection

The power down of the circuit is smooth and free from voltage spikes. When the pulse train is interrupted at the input, the C2 capacitor keeps the input of the CMOS inverter high and R1 discharges C3. By the time the input to the CMOS inverter drops below the threshold voltage of Q4, C3 is completely discharged the output remains low.

The addition of a MOS-Gate Driver IC improves the performance of the circuit in Figure 24a, at the expenses of prop delay. The circuit shown in Figure 26a has the following features:

- No secondary supply required
- Propagation delay ~500ns (CL= 10nF)
- Duty cycle range 5% to 85%
- Nominal operating frequency 50kHz (20kHz to 100kHz)
- Short circuit protection with Vce sensing. Threshold Vce = 7.5V
- Undervoltage lock-out at Vcc = 9.5V
- Over voltage lock out at Vcc = 20V

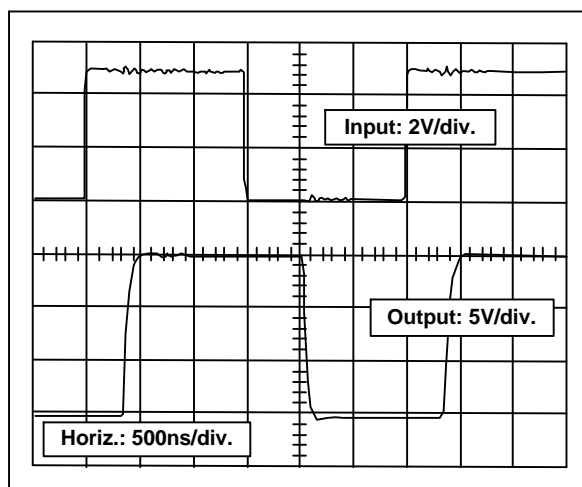


Figure 26b. Waveforms associated with the circuit of Figure 26a.

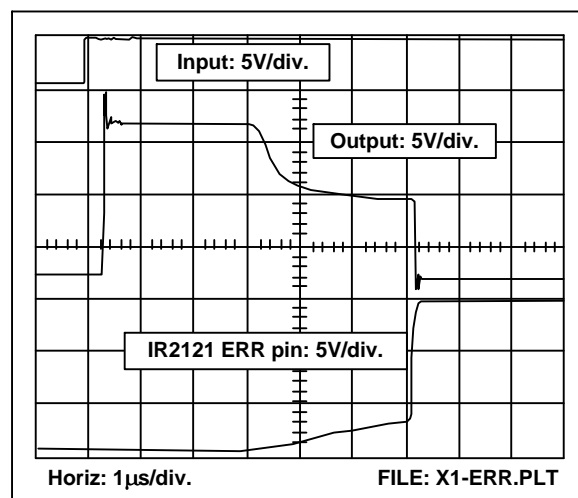


Figure 27. Shutdown due to high V_{CEsat}

The short circuit protection is implemented with a Vce sensing circuit in combination with the current sense input (CS) of IR2127/8. When the HO pin of U2 goes high R3 starts charging C5. Meanwhile the IGBT turns on, the collector voltage drops to the saturation level, D5 goes into conduction and C5 discharges. When the collector voltage is high, D5 is reverse biased and the voltage on C5 keeps raising. When C5 voltage exceeds 250mV the IR2127/8 shuts down the output. The fault to shut-down delay is approximately 2 microseconds.

For operation with a large duty cycle, several options are available. The circuits described in AN-950 use a saturating transformer to transfer the drive charge to the gate. The circuit shown in Figure 28a, on the other hand, achieves operation over a wide range of duty cycles by using the MGD as a latch. It has the following features:

- Frequency range from DC to 900kHz.
- Turn-on delay: 250ns.
- Turn-off delay 200ns
- Duty cycle range from 1% to 99% at 100kHz.
- Under voltage and over voltage lockout.
- Optional short circuit protection, as shown in Figure 26a

In the circuit of Figure 28a the transformer is small (8 turns), since it transmits only short pulses to the secondary side. The MGD on the secondary side of the transformer is latched by the feedback resistor R4. Figures 28b and 28c show the performance of this circuit at the two extremes of 900 kHz and 2.5 Hz

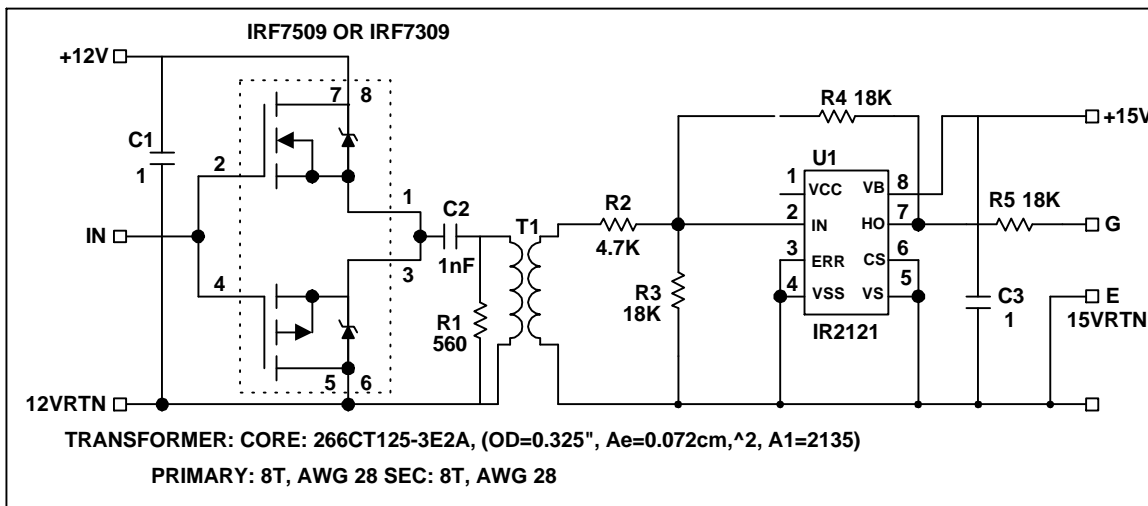


Figure 28a. Transformer-coupled MGD for operation from DC to 900 kHz

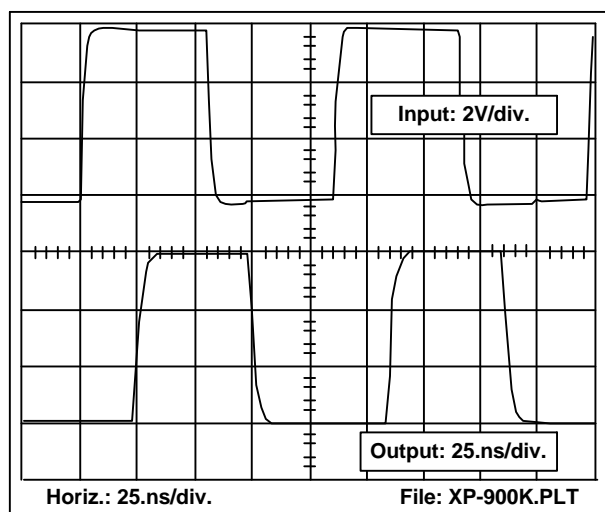


Figure 28b. Waveforms associated with the circuit of Figure 28a operated at 900 kHz

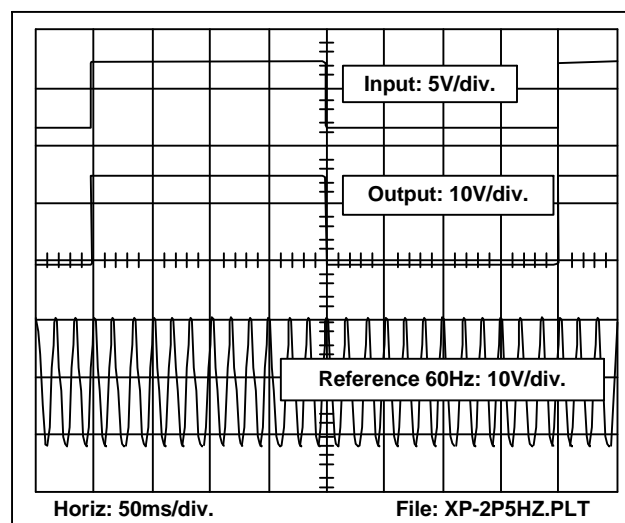


Figure 28c. Waveforms associated with the circuit of Figure 28a operated at 2.5 Hz

7.2 Chopping gate drives

Chopper circuits can maintain a gate drive signal for an indefinite period of time, have good noise immunity performance and, with some additional circuitry, the isolated supply can be avoided.

The basic operating principle is shown in Figure 29. To turn on the MOSFET, a burst of high frequency is transmitted to the secondary side. The MOSFET is turned off by interrupting the high frequency. The diode and the bipolar transistor form a crowbar that rapidly discharges the gate.

In addition to providing the gate drive signal, the high frequency transformer is frequently used to power auxiliary circuitry, like short-circuit protection, thus avoiding a dedicated supply.

8. DRIVE REQUIREMENTS AND SWITCHING CHARACTERISTICS OF LOGIC LEVEL HEXFET[®]S

Many applications require a power MOSFET to be driven directly from 5 V logic circuitry. The on-resistance of standard power MOSFETs is specified at 10 V gate drive, and are generally not suitable for direct interfacing to 5V logic unless an oversized MOSFET is employed.

Logic level HEXFET[®]s are specifically designed for operation from 5V logic and have guaranteed on-resistance at 5 or 4.5 V gate voltage. Some have guaranteed on-resistance at 2.7 V.

Some important considerations for driving logic level HEXFET[®]s are discussed in this section and typical switching performance of these is illustrated when driven by some common logic drive circuits.

8.1 Comparison to Standard HEXFET[®]s

Some devices are available as Logic-level HEXFET[®]s as well as standard HEXFET[®]s. The logic-level version uses a thinner gate oxide and different doping concentrations. This has the following effects on the input characteristics:

- Gate Threshold voltage is lower.
- Transconductance is higher.
- Input capacitance is higher.
- Gate-source breakdown voltage is lower.

While input characteristics are different, reverse transfer capacitance, on-resistance, drain-source breakdown voltage, avalanche energy rating, and output capacitance are all essentially the same. Table 3 summarizes the essential comparisons between standard and logic level HEXFET[®]s.

Characteristics and Ratings		Standard HEXFET [®] (IRF Series)	Comparable Logic Level HEXFET [®] (IRL Series)
Gate Threshold Voltage	$V_{GS(on)}$	2 - 4V	1 - 2V
On-Resistance	$R_{DS(on)}$	Logic level HEXFET [®] has same value of $R_{DS(on)}$ $V_{GS} = 5V$ as standard HEXFET [®] at $V_{GS} = 10V$ $R_{DS(on)}$ of logic level HEXFET [®] also speed at $V_{GS} = 4V$	
Transconductance	g_{fs}	Typically 39% larger for logic level HEXFET [®]	
Input Capacitance	C_{rs}	Typically 33% larger for logic level HEXFET [®]	
Output Capacitance	C_{rss}	Essentially the same	
Reverse Transfer Capacitance	C_{rss}	Essentially the same	
Gate Charge			
Gate-Source	Q_{gs}	Essentially the same	
Gate-Drain	Q_{gd}	Essentially the same	
Total	Q_g	Essentially same as $V_{GS} = 10V$	Essentially same at $V_{GS} = 5V$
Drain Source Breakdown Voltage	BV_{DSS}	Same	
Continuous Drain Current	I_D	Same	
Single Pulse Avalanche Energy	E_{AS}	Same	
Max. Gate-Source Voltage	V_{GS}	$\pm 20V$	$\pm 10V$

Table 3: Essential Comparisons of Standard and Logic Level HEXFET[®]s

The gate charge for full enhancement of the logic level HEXFET[®] is, however, about the same as for a standard HEXFET[®] because the higher input capacitance is counteracted by lower threshold voltage and higher transconductance. Since the logic level HEXFET[®] needs only one half the gate voltage, the drive energy is only about one half of that needed for the standard HEXFET[®]. Since the gate voltage is halved, the gate drive resistance needed to deliver the gate charge in a given time is also halved, relative to a standard HEXFET[®]. In other words, for the same switching speed as a standard HEXFET[®] power MOSFET, the drive circuit impedance for the logic level HEXFET[®] must be approximately halved.

The equivalence of switching times at one half the gate resistance for the logic level HEXFET[®] is illustrated by the typical switching times for the IRL540 and the IRF540 HEXFET[®]s shown in Table 4, using data sheet test conditions.

Gate Resistance R_G (Ω)	Gate Voltage V_{GS} (V)	Drain Current I_D (A)	Typical Values (ns)			
			$t_{D\ on}$	t_r	$t_{D\ on}$	t_r
9	10	28	15	72	40	50
4.5	5	28	15	72	44	56

Table 4: Typical Resistive Switching Times for IRL540 and IRF540

TTL families do not actually deliver 5V in their V_{OH} condition, even into an open circuit. The 5V level can, however, be reached by the addition of a pull-up resistor from the output pin to the 5V bus, as illustrated in Figure 30. Without the pull-up resistor, the $R_{DS(on)}$ value at $V_{GS} = 5V$ may not be attained, and the value specified at $V_{GS} = 4V$ should be used for worst case design.

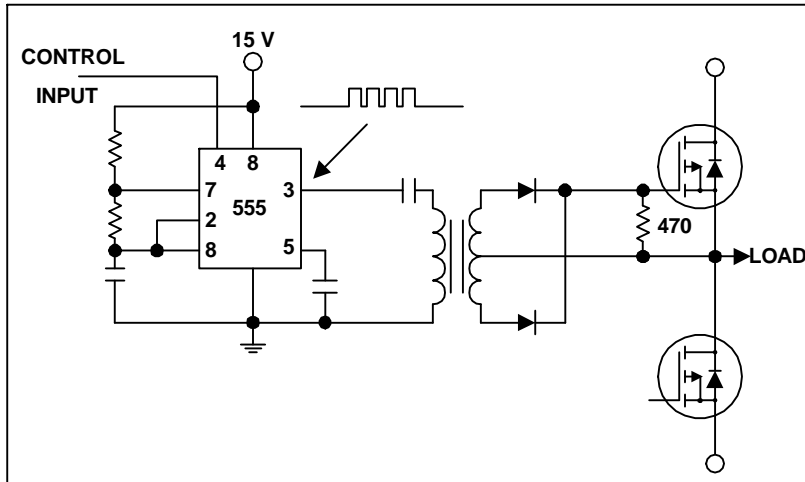


Figure 29.

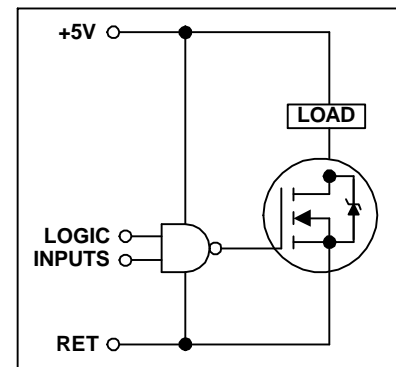


Figure 30. Pull-up resistor used to deliver 5V gate drive

8.2 Driving Logic Level HEXFET[®]s

The gate threshold voltage of MOSFETs decreases with temperature. At high temperature it can approach the $V_{OL(max)}$ specification of the logic driver. Care should be exercised to insure that $V_{TH(min)}$ at the highest operating temperature is greater than $V_{OL(max)}$ of the various logic families in order to guarantee complete turn off.

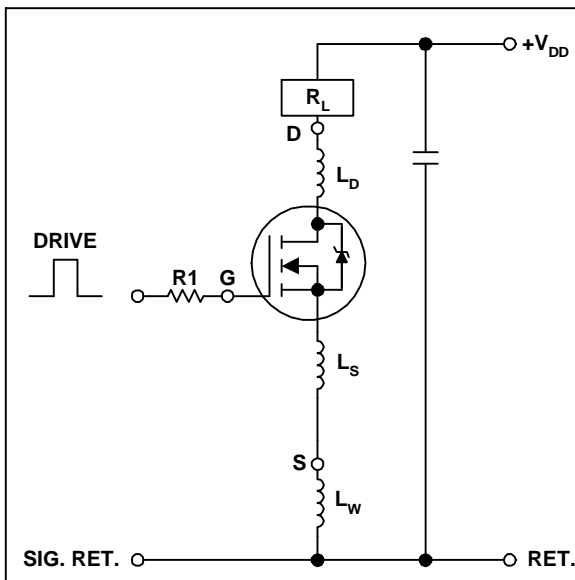


Figure 31a. High common mode inductance

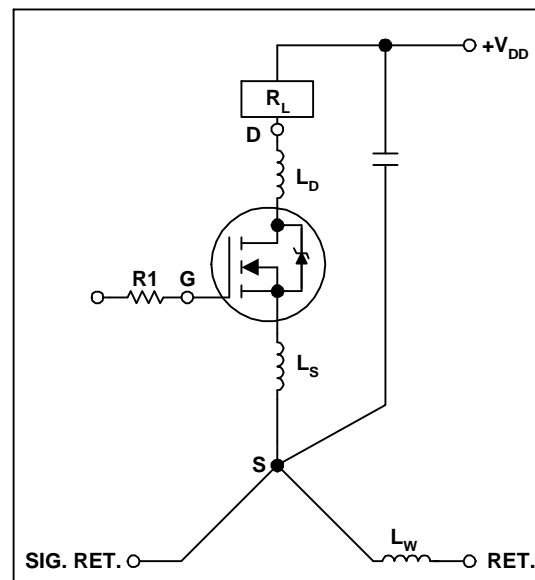


Figure 31b. Minimum common mode inductance

Common source inductance plays a significant role in switching performance. In the circuit of Figure 31a the switching performance is degraded due to the fact that V_{GS} is reduced by $(L_S + L_W) di/dt$, where di/dt is the rate of change of the drain current. By eliminating L_W from the drive circuit, V_{GS} can approach the applied drive voltage because only L_S (the internal source inductance) is common.

This can be done by separately connecting the power return and the drive signal return to the source pin of the switching HEXFET[®], as shown in Figure 31b. Thus, the load current I_D does not flow through any of the external wiring of the drive circuit; consequently, only the internal source inductance L_S is common to both load and drive circuits.

In the case of logic level HEXFET[®]s, for which V_{GS} is 5V and not 10V, the loss of drive voltage due to common mode inductance has proportionately twice the effect as it would on a 10V drive signal, even though actual values of L_S and L_W are the same.

8.3 Resistive Switching Tests

In the following tests of switching performance, the physical layout of the test circuit was carefully executed so to minimize the common source inductance. The following precautions were also observed:

1. R_L was built by paralleling 0.5W resistors to achieve the desired load resistance (see Table 5).
2. To minimize inductance in the load circuit, a 10 μ F low-ESR low-ESL capacitor was connected directly from $+V_{DD}$ to the source of the DUT.
3. To provide a low source impedance for the 5V gate pulse of the DUT, a 0.1 μ F low-ESR low-ESL capacitor was connected directly between pin 14 and pin 7 of the driver IC.
4. To provide minimum common source impedance, the source of the DUT was the common return point of all ac and dc system grounds.
5. To reduce stray inductances and thus achieve maximum switching speeds, the physical size of the high current loop (R_L , DUT, 10 μ F) was reduced to the smallest practical limits.

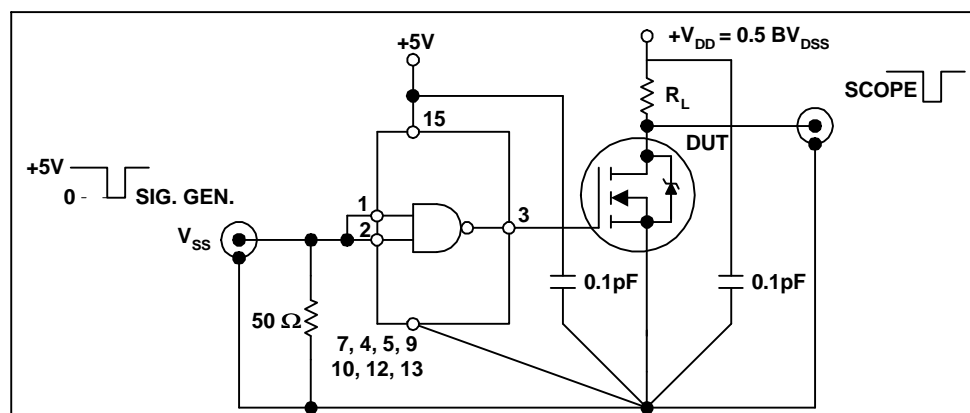


Figure 32. Switching test circuit. Logic level driver is one-quarter of a quad NAND gate.

Only the 5 volt families have been tested as logic level HEXFET[®] drives: bipolar and CMOS (and their derivatives), as indicated below.

TTL GATES

DM7400N:	Standard TTL
74F00PC:	High Speed TTL
DM74S00N:	Schottky TTL
DM74LS00N:	Low Power Schottky TTL
DM74AS00N:	Advanced Schottky TTL

CMOS GATES

74AC00PC:	Advanced CMOS
74ACT00PC:	TTL Compatible CMOS
MM74HC00N:	Micro CMOS
MM74HCT00N:	TTL Compatible Micro CMOS

BIPOLAR

DS0026: High Speed MOSFET Driver

The test conditions for the resistive switching performance is shown in Table 5. The resistive switching times obtained with the above TTL and CMOS gates are tabulated in Table 6. In this table t_{on} = Time in microseconds from 90% to 10% V_{DD} and t_{off} = Time in microseconds from 10% to 90% V_{DD} . Inductive switching gives faster voltage rise times than resistive switching due to the resonant charging of the output capacitance of the device. Voltage fall times are essentially the same.

LOGIC LEVEL HEXFET [®]	SWITCHING VOLTAGE (V)	SWITCHING CURRENT (A)	R _{DS(on)} (Ω)	R _L (Ω)
IRLZ14	30	8	0.24	3.25
IRLZ24	30	16	0.12	1.5
IRLZ34	30	24	0.06	1.2
IRLZ44	30	40	0.034	0.7
IRLZ514	50	5	0.60	9.5
IRLZ524	50	8	0.30	5.9
IRLZ524	50	12	0.18	4.0
IRLZ544	50	25	0.085	1.9

Table 5. Resistive Switching Conditions

Logic Family	Logic Level HEXFET [®]																	
	Quad, Dual Input		IRLZ14		IRLZ24		IRLZ34		IRLZ44		IRL514		IRL524		IRL534		IRL544	
Nand Gate	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}
DM7400N STANDARD TTL	0.173	0.018	0.663	0.026	0.700	0.076	1.491	0.146	0.151	0.022	0.238	0.041	0.263	0.060	0.616	0.124		
7400FDOPC HIGH SPEED TTL	0.124	0.008	0.490	0.013	0.429	0.068	0.863	0.146	0.104	0.004	0.159	0.034	0.176	0.059	0.372	0.136		
DM7400 SCHOTTKY TTL	0.133	0.092	0.549	0.020	0.503	0.032	1.068	0.142	0.116	0.006	0.183	0.041	0.212	0.057	0.441	0.132		
DM74LS LOW POWER SCHOTTKY TTL	0.174	0.038	0.778	0.093	0.706	0.146	1.438	0.342	0.155	0.040	0.240	0.062	0.267	0.090	0.567	0.199		
DM4SDON ADVANCED SCHOTTKY TTL	0.126	0.008	0.567	0.013	0.446	0.023	0.896	0.149	0.111	0.005	0.161	0.127	0.176	0.058	0.336	0.130		
74ACOOPC ADVANCED CMOS	0.012	0.007	0.120	0.012	0.125	0.027	0.251	0.139	0.036	0.004	0.052	0.028	0.066	0.055	0.125	0.125		
74ACTOOPC TTL COMPATIBLE CMOS	0.012	0.006	0.121	0.011	0.125	0.016	0.233	0.127	0.033	0.044	0.052	0.027	0.060	0.055	0.120	0.122		
MM74CHCOON MICRO CMOS	0.066	0.039	0.179	0.091	0.227	0.147	0.508	0.328	0.058	0.044	0.092	0.068	0.111	0.096	0.232	0.213		
MM74HCTCO4 TTL COMPATIBLE MICRO CMOS	0.066	0.030	0.179	0.060	0.227	0.123	0.504	0.269	0.068	0.035	0.092	0.051	0.111	0.086	0.232	0.186		
DS0026 HIGH SPEED MOSFET DRIVER	0.052	0.005	0.016	0.005	0.014	0.007	0.032	0.016	0.021	0.004	0.036	0.004	0.036	0.005	0.029	0.009		

Table 6. Results of the resistive load switching test

Typical Test Oscilloscopes

IRLZ24: 60V, 0.1 Ohm, N-Channel, TO-220 logic level HEXFET[®] was driven by each of the logic families listed in Table 4 and the comparative resistive switching times photographed.

9. SIMPLE AND INEXPENSIVE METHODS TO GENERATE ISOLATED GATE DRIVE SUPPLIES

In several applications, dc-to-dc converters are used to power the MOS Gate Driver. Although the gate drive requires little power, the noisy environment, the isolation voltage and creepage distance requirements and the high dv/dt between the primary and secondary size make the design of the DC-to-DC converter somewhat complicated. Its key parameters are listed below: OUTPUT VOLTAGE, CURRENT. The output voltage of the DC-to-DC converter is the sum of the positive and negative drive voltage to the gate. The load current required from the DC-to-DC converter is the sum of the current consumption of the drive circuit and the average drive current to the gate.

dv/dt CAPABILITY. When the DC-DC converter powers a high side switch, the secondary side of the converter is connected to the output of the power circuit. The rapid change of high voltage at the output of power circuit stresses the isolation of the transformer and injects noise to the primary side of the transformer. Switching noise at the primary side disturbs the operation of the converter and the control circuit for the power stage, causing false triggering and shoot-through. Therefore a transformer with high voltage isolation, appropriate creepage distances and low winding-to-winding capacitance is required in this application.

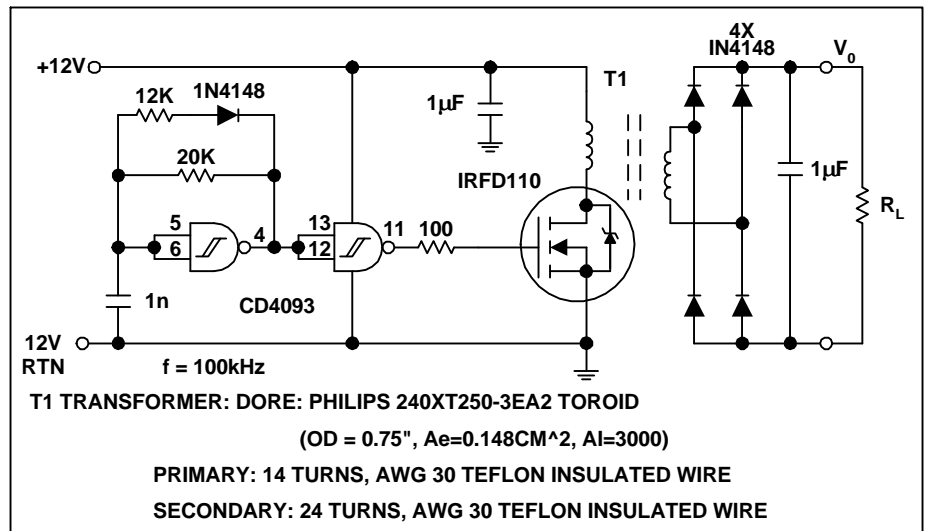


Figure 33a. 100 kHz Forward converter

SMALL SIZE. To reduce the interwinding capacitances the transformer must be made small. This implies operation at high frequency. Small size and compact layout help reducing the EMI and RFI generated by the converter. Figure 33a shows a forward converter made with two CD4093 gates to generate the clock and drive the MOSFET. Energy as transferred to the secondary when the MOSFET is on, in about 33% of the cycle. When the MOSFET is off, the secondary winding is used to demagnetize the transformer and transfer the magnetizing energy to the load, thus eliminating the need for a demagnetizing winding. The switching waveforms are shown in Figure 33b. The ringing in the drain voltage during the fly-back period is due to the loose coupling between the primary and the secondary windings. The load current vs. output voltage characteristic of the circuit is shown in Figure 34. When the output current falls below 5 mA, the circuit works as flyback converter because the demagnetizing current flows through the output. A minimum load of 5mA is required to limit the output voltage at 15V.

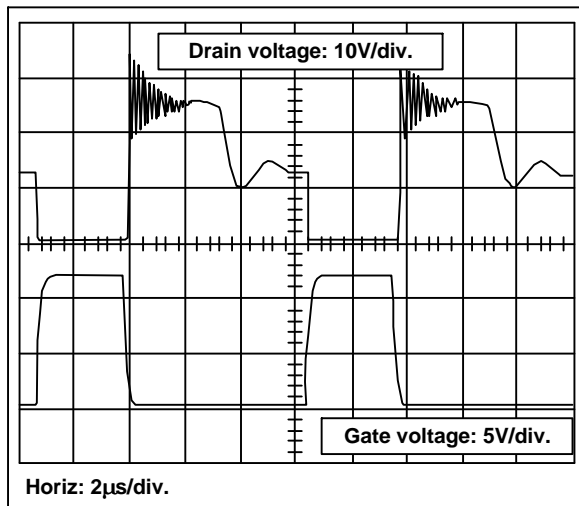


Figure 33b. Waveforms associated with the circuit in Figure 33a

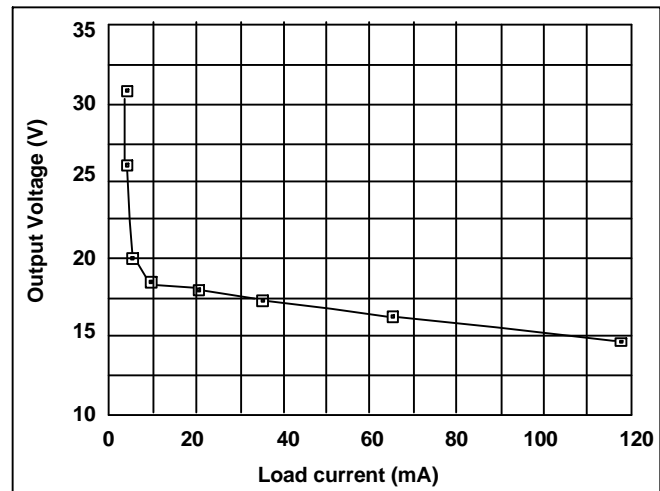


Figure 34. Load current vs. output voltage at 100 kHz, $R_{out} = 27.7$ Ohms

If the converter is loaded with a constant and predictable load, a zener can provide the necessary regulation. Otherwise a three-terminal regulator or a small zener-driven MOSFET may be necessary.

The circuit in Figure 35a is similar to the previous one, except that the higher switching frequency is higher (500 kHz) and the transformer is smaller. The remaining three gates in the package are connected in parallel to drive the MOSFET and reduce the switching losses. The switching waveforms are shown in Figure 35b. The output resistance (R_{out}) of this circuit is higher than the circuit shown in Figure 33a, mainly because the stray inductance of the smaller transformer is higher and the effects of the stray inductance are higher. Figure 37a shows a push-pull operated at 500 kHz. The single gate oscillator produces a 50% duty cycle output, while the remaining gates in the package are used to drive the push-pull output stage. The primary of the transformer sees half the voltage compared to the previous circuit, therefore the number of turns at the primary were reduced to half.

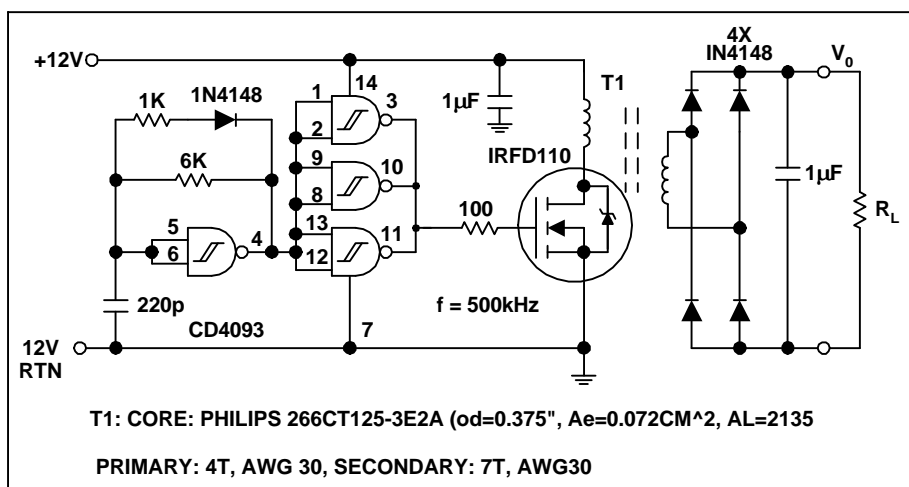


Figure 35a. 500 kHz Forward converter

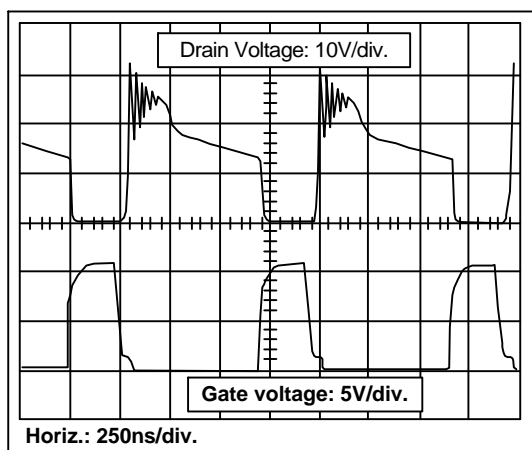


Figure 35b. Waveforms associated with the circuit in Figure 35a

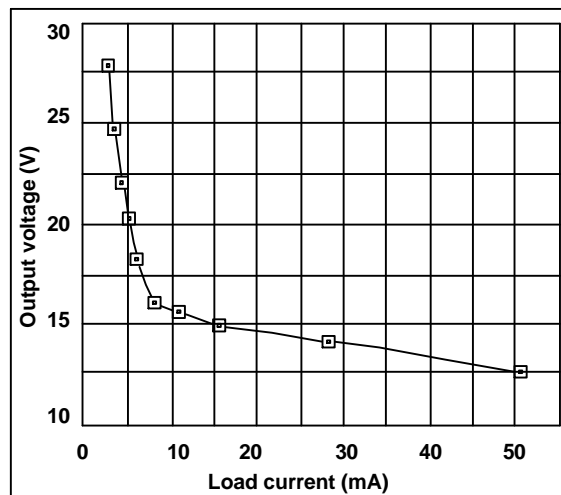


Figure 36. Load current vs. output voltage, $R_{out} = 27.7$ Ohms

10. PHOTOVOLTAIC GENERATORS AS GATE DRIVERS

A photovoltaic generator is a solid state power supply powered by light, normally an LED. The combination of the LED and the photovoltaic generator in one package is called a Photovoltaic Isolator or PVI and is available in a 8-pin DIP package. As a voltage source, the PVI can function as a "dc transformer" by providing an isolated low current to a load. While an optoisolator requires a bias supply to transmit a signal across a galvanic barrier, the PVI actually transmits the energy across the barrier. More information on the PVI can be found in Application Note GBAN-PVI-1 which appears in the Microelectronic Relay Designer's Manual. This data book also contains the data sheet for the photovoltaic isolator, the PVII050. A circuit is also provided in the AN to significantly speed up turn off of the switch. As a gate driver the PVI has significant limitations: its short circuit current is in the order of 30 microA with a very high internal impedance. Its simplicity, however, makes it appealing in solid-state relay replacements, where switching times are not important and switching transients are not present.

A typical application is the ac switch described below. The IGBT and the power MOSFET are not suited to switching AC waveforms directly. The IGBT can only conduct current in one direction while the power MOSFET has an anti-parallel diode that will conduct during every negative half-cycle. Bidirectional blocking capability can be achieved by connecting two power MOSFETs source to source, or two IGBTs with anti-parallel diodes emitter to emitter, as shown in Figure 39.

In the case of the MOSFET, there is the possibility that, for low current levels, the current flows through both MOSFET channels, instead that one MOSFETs and diode, thereby achieving lower overall voltage drop. The MOSFET channel is a bidirectional switch, that is, it can conduct current in the reverse direction.

If the voltage across the MOSFET channel is less than the VF of the intrinsic diode (which typically has a higher VF than discrete diodes), then the majority of the current will flow through the MOSFET channel instead of the intrinsic diode. The gate drive for both the MOSFETs and IGBTs must be referenced to the common sources or emitters of the devices. Since this node will be swinging with the AC waveform, an isolated drive is necessary. The PVI can be used, as shown in Figure 40.

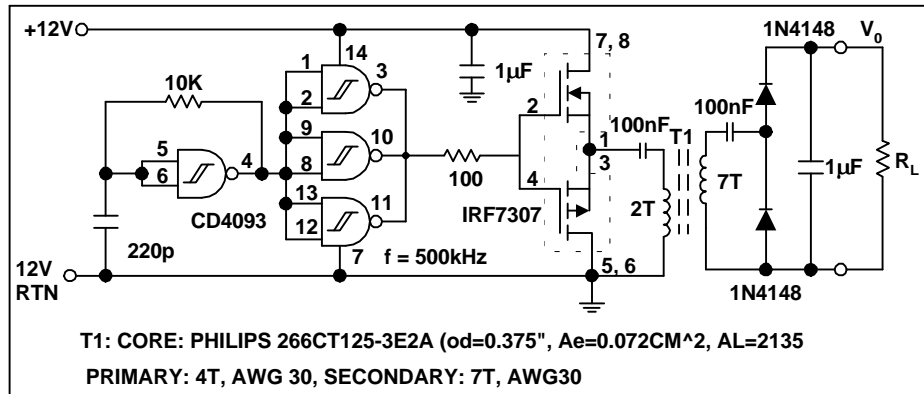


Figure 37a. 500 kHz Forward converter

11. RESONANT GATE DRIVE TECHNIQUES

As indicated in Section 14, gate drive losses in hard switching are equal to $Q_{gs} \times V_{gs} \times f$. An IRF630 operated at 10 Mhz with a gate voltage of 12 V would have *gate drive losses* of 3.6 W, independent from the value of the gate drive resistor. Clearly, to achieve hard switching at this frequency, the resistance of the gate drive circuit is limited to whatever is associated with the internal impedance of the driver and with the gate structure of the device itself. Furthermore, the stray inductance of the gate drive circuit must be limited to tens of nH. The design and layout of such a circuit is not an easy task.

An alternative method to drive the gate in such an application is to design a resonant circuit that makes use of the gate capacitance and stray inductance as its reactive components, adding whatever inductance is necessary to achieve resonance at the desired frequency. This method can reduce the peak of the gate drive current and losses in half, while simplifying the design of the gate drive circuit itself. Since the gate charge is not dissipated at every switching transition, but stored in a reactive component, the gate drive losses are proportional to the resistance of the gate drive circuit, rather than being independent from it. More information on this gate drive method can be found in an article by El-Hamamsy: Design of High-Efficiency RF Class-D Power Amplifier and in references at the end of this article (IEEE Transactions on Power Electronics, May 1994, page 297).

Related Topics

- MOS-Gate Driver Ics
- Transformer drive with wide duty cycle capability
- Gate Charge
- Three-phase MOS-Gate Driver
- Photovoltaic Isolators (PVI)

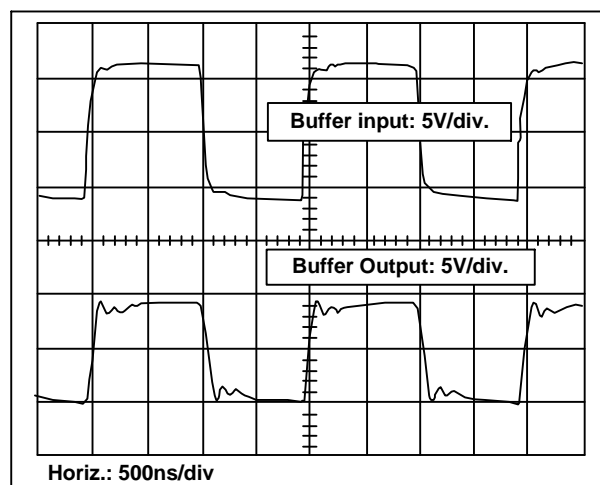


Figure 37b. Waveforms associated with the circuit in Figure 37a

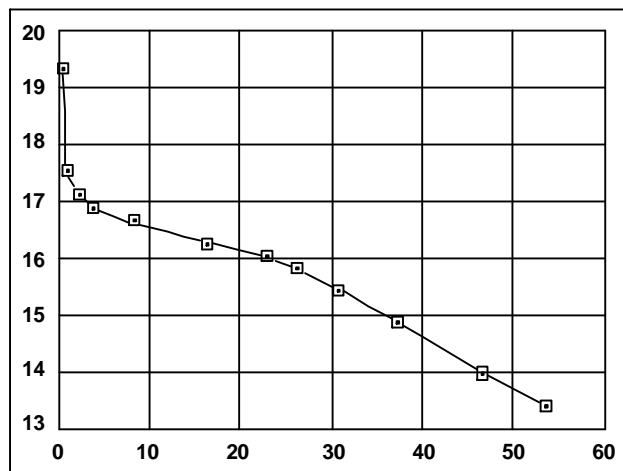


Figure 38. Load current vs. output voltage,
 $R_{out}=27.7$ Ohms

Mounting Considerations For International Rectifier's Power Semiconductor Packages

by Pamela Dugdale and Arthur Woodworth, International Rectifier

Introduction

It is important that power semiconductors are correctly mounted if full functionality is to be achieved. Incorrect mounting may lead to both thermal and mechanical problems. The aim of this Application Note is to describe good practise in the mounting of power semiconductors.

Making Good Thermal Contact

One of the major considerations when mounting all power semiconductor packages is the dissipation of heat. This is because the junction temperature of the die and the glass transition temperature of the plastic limit the performance of the device. Indeed there are maximum allowable temperatures above which the device functionality cannot be guaranteed. The way in which a device is mounted can have a large effect on the thermal contact between the header and the heat sink and hence on the ability of the package to dissipate heat. This is often referred to as the contact thermal resistance and is quoted in datasheets. A full discussion of all of the components that make up the thermal resistance of a power semiconductor package is given in International Rectifier Application Note [AN-997](#) "Mounting Guidelines for the Super-247". In the present note we shall concentrate on the thermal resistance between the case and the heat sink as this is the most dependent on the mounting technique.

The physical source of the contact resistance is a result of the fact that surfaces are never perfectly flat. The recommended flatness for the mounting surface is 0.02mm in 10mm. Particular attention should be paid to ensuring that no damage occurs during the manufacture of mounting holes. Even for two well-prepared surfaces contact only actually occurs at several points separated by large air gaps. This is shown in Figure 1. As air is a very good thermal insulator this is undesirable and increases the thermal resistance. There are two ways of reducing the volume of air trapped between the surfaces. One is to increase the force holding the two surfaces together and the other is to improve the quality of the contact area by filling in the gaps. In the case of the former this can be done by either applying a force above the die with a clip or by increasing the torque on the screw, which mounts the tab to the heatsink. The way in which the thermal resistance varies as a function of the torque on the mounting screw or the clip force is shown in Figs. 2 and 3. Over tightening the mounting screw may lead to deformation of the semiconductor package and hence an increase in the thermal resistance. This is shown in Fig. 2 which gives the thermal resistance as a function of torque for the PowIRtab™, showing a minimum at 1.1Nm for dry mounting and 0.8Nm for wet mounting. Other package types behave in a similar way. Details of how to correctly mount down a semiconductor to avoid this and other problems are given in this application note.

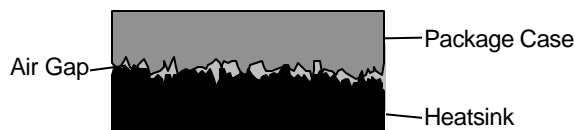


Figure 1. Cross section showing the source of the thermal contact resistance between a package case and the heat sink.

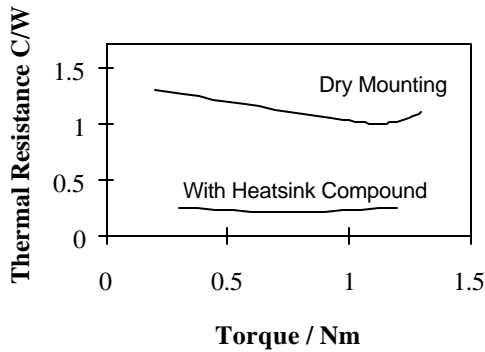


Figure 2. Contact thermal resistance as a function of mounting screw torque for a PowIRtab™ package mounted to a heat sink showing both dry mounting and mounting using heat sink compound.

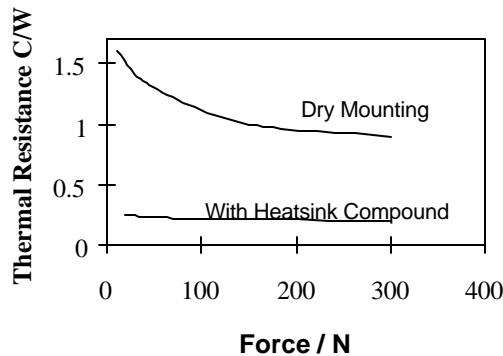


Figure 3. Contact thermal resistance as a function of clip force for a PowIRtab™ package mounted to a heat sink showing both dry mounting and mounting using heat sink compound.

The second technique requires the use of a heat sinking compound. This is usually a silicone grease loaded with electrically insulating, thermally conductive material such as alumina. The purpose of the grease is to fill the gaps without increasing the distance between the two surfaces. If the layer of grease is too thick then the thermal resistance will be increased. To determine the correct amount of grease for a particular application a series of experiments should be performed. Several power packages and heat sinks should be assembled using different amounts of grease applied evenly to one side of each mounting surface. This can be achieved using a small rubber roller. When the amount is correct a very small amount of grease should appear around the perimeter of the device

as it is slowly torqued or clip mounted to the heat sink. Excess compound should be carefully removed.

An alternative to grease is the use of thermally conductive pads. These are conformal under pressure and tend to fill the air voids in the same way as grease. The main advantage of this approach is the ease of handling, however as many of these pads are silicone based the thermal resistance of this solution tends to be higher than it would be if grease were used. In addition to this, the silicone pads provide electrical isolation, which can be either an advantage or disadvantage depending on the specific application. An alternative approach is to use a phase change material. These materials are solid until they are heated to temperatures in the range 50°C to 60°C at which point they start to flow, filling the air gaps. Such materials are available on their own or as coatings on silicone or other thermally conductive pads. For the case when electrical isolation is not required, the phase change material is available as a thin coating on aluminium foil. The relative performance of thermal grease, phase change materials and silicone conductive pads and is given in Table 1. These results were measured by International Rectifier engineers at the Assembly R&D lab.

Interface Material	Electrical Properties	Thermal Resistance Junction to Heat Sink
Heat sink Compound	Non - Conducting	0.7°C/W
Phase Change Thermal Compound	Non - Conducting	1.2°C/W
Aluminium Foil Coated in Phase Change Compound	Conducting	1.2°C/W
Thermal Interface Pad	Isolating	1.6°C/W
Thermal Interface Pad	Conducting	1.6°C/W

Table 1. Performance of thermal interface materials.

Correct Mounting Procedures

In this section the correct mounting procedures for the TO220 package will be discussed. This will include advice on clip mounting, screw mounting and the requirements for isolation. By

using the TO-220 as an example most of the common issues relating to the mounting of power packages will be covered. Problems that are specific to the other power packages, including the International Rectifier PowIRtab™ and Super packages, will be discussed in the next section.

General Rules

- The TO-220 package should always be fastened to the heat sink before soldering the leads to the PCB.
- When bending the leads they must be clamped tightly between the package and the bending point to avoid strain on the package. The leads must be bent at a minimum distance of 2mm from the plastic for standard packages, and 3mm from the plastic for the TO-273. The TO-274 is not normally lead formed because of the design of the leg.
- The leads should be bent no more than 90° and should never be bent more than once.
- The radius of curvature should not be less than the thickness of the leads and ideally should be greater than 2 times the thickness of the leads.
- Lateral lead forming is not advisable. The pin spacing of the leads should be adhered to when mounting to a PCB.
- It is recommended that in the case where a device is rigidly secured to a PCB and also to a heat sink mounted on the PCB, a bend is put in the leads to allow for differences in thermal expansion.
- Care should be taken not to cause any mechanical damage to the package or any surface finishes.
- Heat sink compound or some other thermal interface material should be used.

Screw Mounting

- For the TO-220 a M3 screw should be used. Self-tapping screws should not be used.
- It is recommended that a rectangular washer is inserted between the screw head and the mounting tab. Care must be taken to ensure that the washer does

not damage the plastic body of the package during the mounting process.

- The recommended mounting torque is 1.1Nm. This should not be exceeded.
- When electrical isolation is required insulating pads and insulating bushes should be used.

Figures 4 and 5 show the suggested mounting hardware for the TO-220.

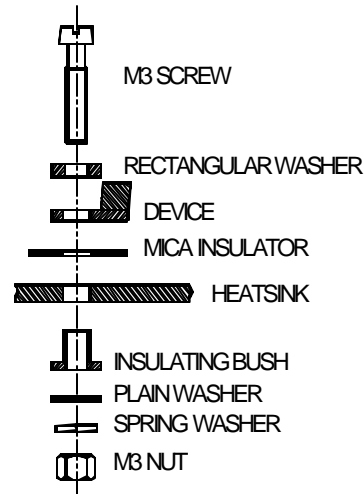


Figure 4. Screw mounting through a heat sink using a nut.

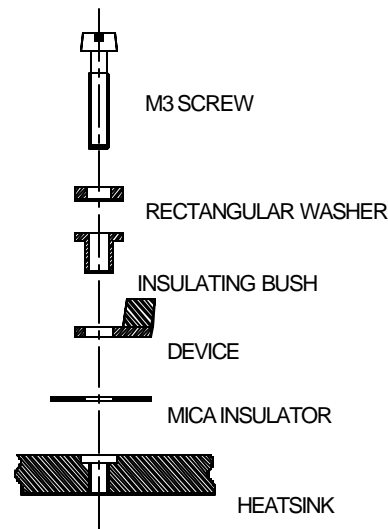


Figure 5. Screw mounting into a tapped heat sink.

Clip Mounting

This section is applicable to the TO-220 and Super220™ (TO-273) packages.

- Using clip mounting ensures that the force is applied above the silicon and that the thermal contact is good.

Application of force off-centre (i.e. bolting a device to heatsink) leads to uneven thermal contact. Using clip mounting ensures that the force is applied above the silicon and that the thermal contact is good.

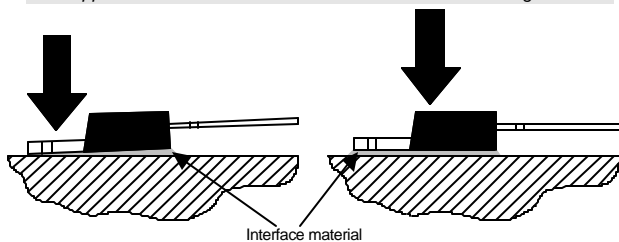


Figure 6. The effect of the position of the applied force.

- Increasing the force supplied by the clip will ensure reduced thermal resistance. This is shown in Figure 3. However the increased cost of stronger clips is not always worth the performance improvements and a minimum force of 20N and typically up to 50N is recommended.
- Isolation is safely achieved by the use of an insulating pad and without the use of bushes.
- Isolation between the bond wires and the mounting clip is provided by the mould compound. The minimum thickness of plastic between a bond wire and the clip is greater than the thickness of the plastic on the header of a fullpak device. This provides 4kV dc isolation which is equivalent to 2.5kV rms ac.
- For heat sinks less than 5mm in thickness saddle clips should be used. These produce contact forces of between 15N and 50N.

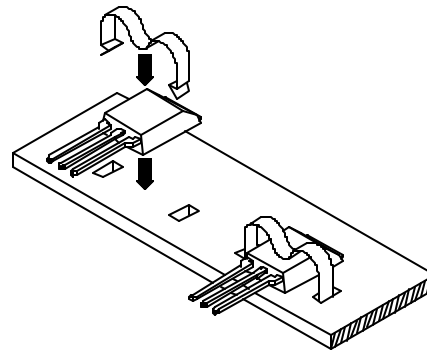


Figure 7. Saddle clip mounting of a Super220™ package.

- For heat sinks greater than 5mm in thickness, U clips are used. These produce contact forces of between 15N and 50N.

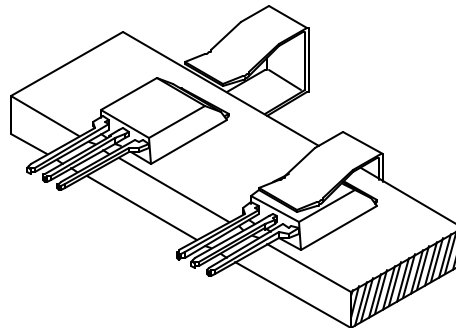


Figure 8. U-Clip mounting of a Super-220™ package.

- There are a number of proprietary clip solutions where the clip is anchored in a feature in an extruded heat sink. Forces of between 25N and 50N can be achieved.

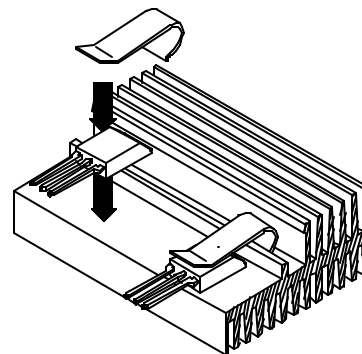


Figure 9. Customized Clip Mounting of a Super-220

Pop Riveting

- It is recommended that press rivets made of a soft material are used rather than pop rivets.
- The hole in the heat sink should be smaller than the device mounting hole, within acceptable tolerances. This ensures that the rivet squeezes more tightly on the heat sink than on the device,

Soldering

A separate application note covers soldering down power semiconductor packages “Surface Mounting of Larger Devices.” In general devices that are being mounted to aluminium heat sinks must be either screw or clip mounted. A new technology, Powersites™, allows solderable power semiconductor packages to be mounted to aluminium heat sinks.

Additional Information for Other Package Types

- Full-Pak devices do not require isolation pads or bushes as the package is isolated by design
- The Super220™ (TO-273) does not have a hole for screw mounting and should be mounted using clips. The ‘hole – free’ design allows the package to carry more current. Full instructions for mounting the Super220™ (TO-273) package are given in [AN-1000](#) “Mounting Guidelines for the Super-220”
- The Super247™ (TO-274) does not have a hole for screw mounting and should be mounted using clips. The ‘hole – free’ design allows the package to carry more current. Full instructions for mounting the Super247™ (TO-274) package are given in [AN-997](#) “Mounting Guidelines for the Super-247”
- Mounting instructions for the PowIRtab package are given in [AN-1010](#) “PowIRtab™ Mounting Guidelines.”
- This is a high current package suitable for mounting to bus bars.

Mounting SOT227

The SOT227 is a power module with some special mounting requirements.



- The package has two mounting holes and four connection terminals.
- Fasten the device to the heat sink before connecting the leads.
- The maximum allowable torque is 1.3Nm on the terminals and on the mounting base.
- M4 screws should be used with lock washers. These are included with the packages.
- The separation of the centre of the mounting holes is 30mm ± 0.2mm. Full details of the dimensions are given on the datasheet.
- The first mounting screw should be tightened to one third of the maximum torque, the second screw should then be tightened to the same torque. Full tightening of both of the screws can then be completed.
- The case to sink thermal resistance at the recommended mounting torque is 0.05C/W for a greased surface.

Links to Suppliers of Thermal Management and Mounting Accessories

<u>Company Name</u>	<u>Link</u>	<u>Suppliers of.....</u>
Aavid Thermal Technologies	www.aavid.com	Interface materials, clips, heatsinks.
Austerlitz Electronic GmbH	www.austerlitz-electronic.com	Interface materials, clips, heatsinks.
Bergquist	www.bergquistcompany.com	Interface materials
Chomerics	www.chomerics.com	Interface materials, PowerSites™, heatspreaders.
Fischerelektronik	www.fischerelektronik.de	Heatsinks and clips.
Fujipoly	www.fujipoly.com	Interface materials
Kunze-Folien	www.kunze-folien.de	Interface materials, clips and customized heat sinks.
R-Theta	www.r-theta.com	Heat sinks
Redpoint Thermalloy	www.thermalloy.com	Interface materials, clips and heatsinks.
Thermagon Inc	www.thermagon.com	Interface materials
Warth International	www.warth.co.uk	Interface materials and clips.

Mounting Guidelines for the SUPER-247

by Andrew Sawle and Arthur Woodworth

Introduction

Born from the need to accommodate ever increasing amounts of silicon in smaller, space saving packages, the SUPER-247 now allows the same die sizes that can be put in a much larger TO-264. The SUPER-247 has the same outer dimensions as the industry standard TO-247 but can dissipate more power than the TO-247 whilst occupying less space than the TO-264. This package also allows the use of efficient and reliable clip mounting methods to heatsinks. This allows designers to reduce both the size and the cost of their systems.

This Application Note will examine the subjects involved with clip mounting the SUPER-247 to heatsinks.

Topics Covered:

A breakdown of system thermal resistance.

The minimum force for a good thermal contact and the maximum force allowable before device parameter degradation.

Wet and dry contact conditions and the effect on thermal resistance.

The effect on thermal resistance of using an electrical isolator between the device and the heatsink.

Typical clip types, how they work and the forces that they impart. Conclusion.

1. A Breakdown of System Thermal Resistance

The thermal resistance ($R_{th(junction-ambient)}$) of a system (system = package through to heatsink) is made up from a number of component parts as shown in Figure 1.1 below.

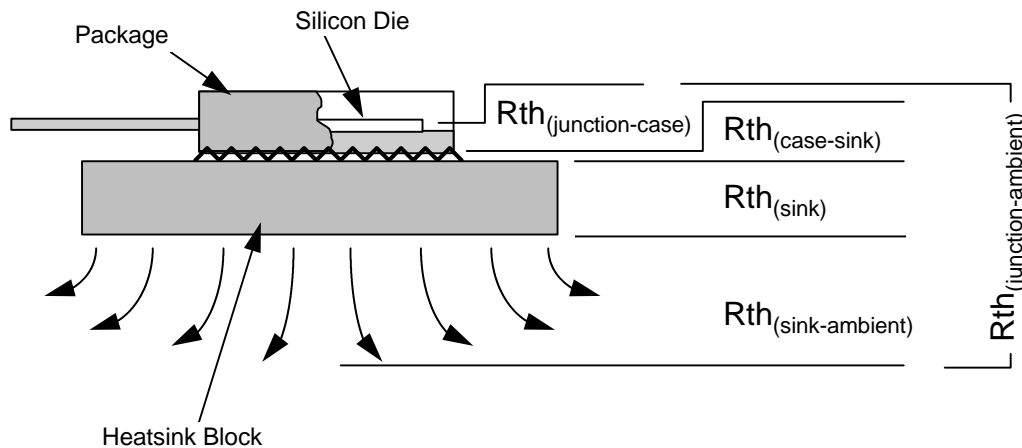


Figure 1.1 - Build-up of Thermal Resistance in a System

The designer of a system has varying amounts of influence over the component parts of the overall thermal resistance of his design:

- $R_{th(junction-case)}$ - this has been determined during the design and manufacture of the product. The system designer has no direct influence.
- $R_{th(case-sink)}$ (or **Contact Thermal Resistance**) - determined by the size and quality of the contact areas between the package and the sink, the use of intermediate materials and the contact pressure. Hence, the system designer can have a large influence over this parameter.
- $R_{th(sink)}$ and $R_{th(sink-ambient)}$ - determined by heatsink design, *i.e. material and shape*. System designer will choose optimum sink matching both performance and cost requirements.

Thermal resistances for packages and heatsinks can be determined from datasheets and although the contact thermal resistances can also be taken from manufacturer's data, this figure is generally 'TYPICAL' and for a single set of specified conditions. Hence, it is possible for a designer to gain better or worse contact thermal resistances depending on parameters that he prescribes. The following sections include some information to help the designer in improving rather than worsening contact thermal resistances in their systems.

2. Minimum and Maximum Contact Forces

As previously mentioned, there are a number of factors that affect the contact thermal resistance, one of the factors being the contact force with which the package is pushed against the heatsink.

Why and How Does Contact Force Affect Thermal Resistance?

Package cases and heatsink surfaces can never be perfectly flat. Hence contact between the two will only occur at several points allowing an air gap between the surfaces (as illustrated in Figure 1.2). Since air is a very good thermal insulator this means that the contact thermal resistance is much greater than it would be if the two surfaces were in perfect contact (no air gap). However, as the contact force (pushing the two surfaces together) increases then so will the number of points at which the two surfaces contact one another and the air-gap will be reduced, in turn reducing the contact thermal resistance.

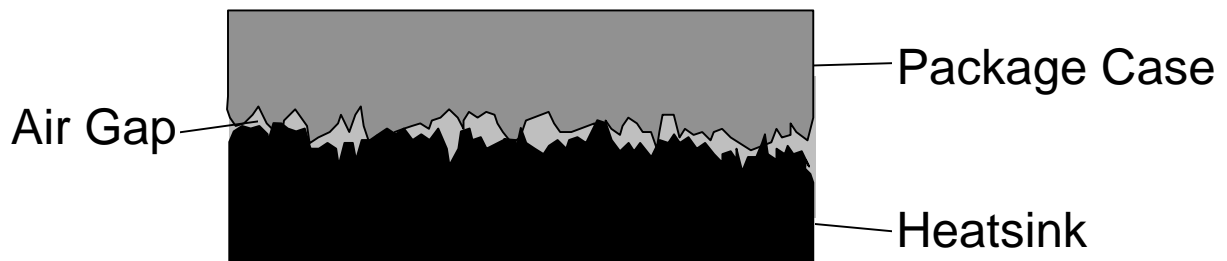


Figure 1.2 - Diagram Showing the Effect (Under High Magnification) When Two Non-Perfect Surfaces Meet.

What is the Minimum Force that Should be Applied to Gain Good Thermal Contact?

As the contact force is increased, the contact thermal resistance decreases. However, this does NOT follow a linear relationship and shows diminishing returns in thermal resistance reduction for increases in the contact force (as shown in Figure 1.3). A rapid initial fall-off in contact thermal resistance is replaced by a more gradual reduction with increased contact force. The minimum contact force should therefore be no lower than the point at which these rapid reductions in thermal resistance end - this occurs at approximately 20N.

Maximum Contact Force

The minimum contact force of 20N mentioned above is purely that, the MINIMUM force. Any force applied above that figure will still show gains in reduced contact thermal resistance until the maximum force that the package can withstand before the device characteristics are altered or the package is destroyed. This maximum limit figure has been measured to be 200N TYP. However, these gains are not free, for in general terms a greater contact force means a larger, more expensive clamping system. A contact force should therefore be chosen that optimises both the thermal and the cost requirements of the system.

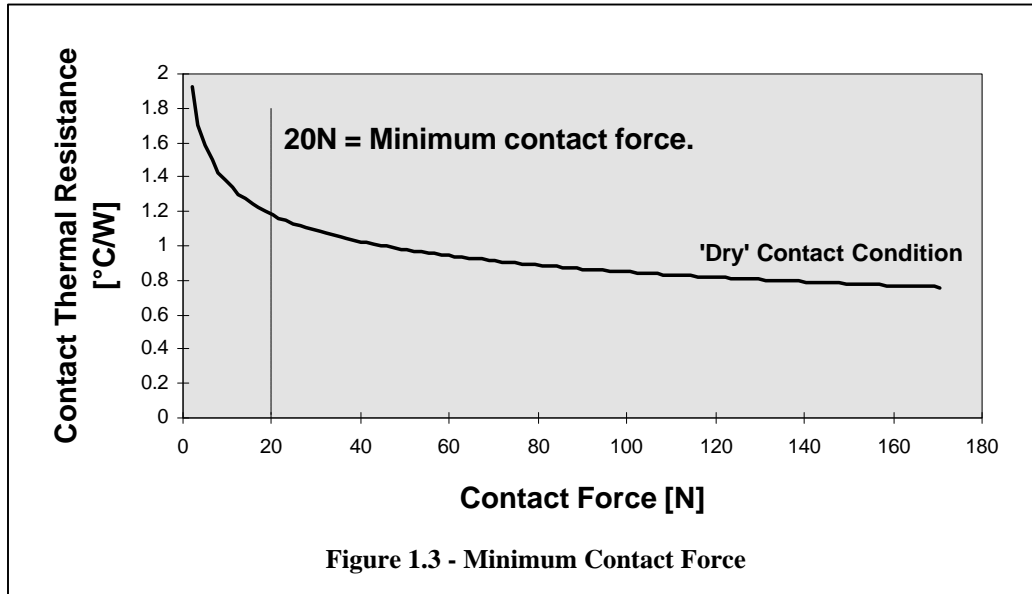


Figure 1.3 - Minimum Contact Force

3. Contact Conditions

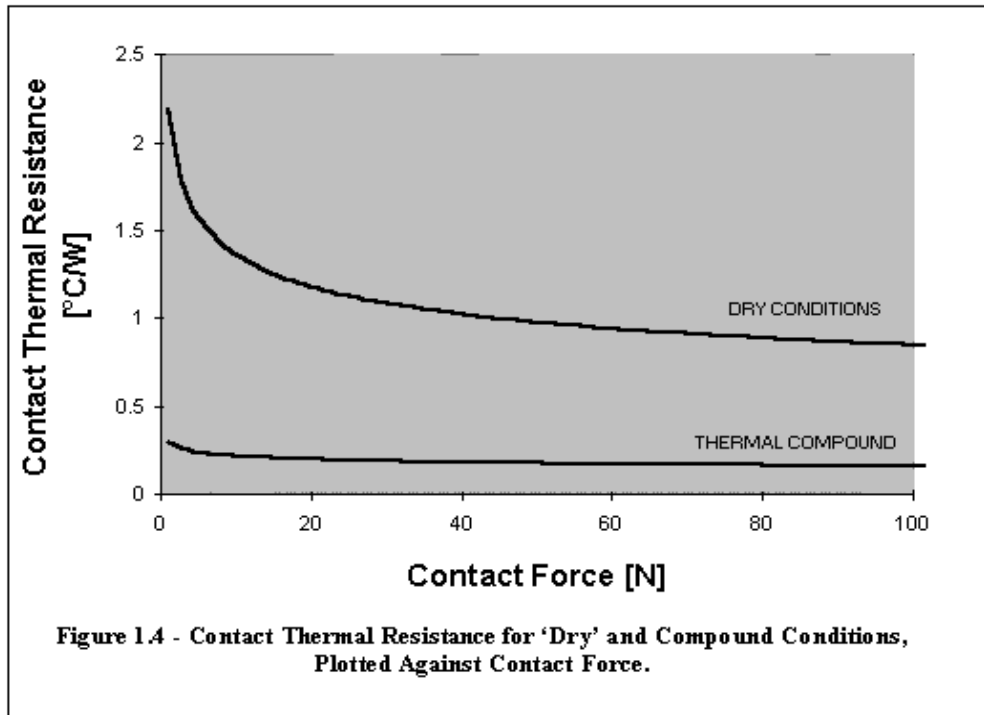
As mentioned previously, the contact conditions between the package and the heatsink will affect the contact thermal resistance. Contact conditions encompass a number of areas including: surface roughness, surface cleanliness, paint finishes and intermediate materials. The surface roughness of the heatsinking material should be no greater than 0.02mm over the area where the device is to be mounted. Surface cleanliness during assembly of package and heatsink is imperative, even if a thermal grease or other material is subsequently added. Unclean surfaces can be held apart by dirt or grease thus increasing the thermal resistance. However, normal paint finishes (up to 50 μm thick) have been shown to have little effect on thermal resistance, this therefore leaves intermediate materials as an area for discussion.

Intermediate Materials

Contact between two non-perfect surfaces will result in an air gap between them. The most common method of overcoming this is to use a thermally conductive heatsinking compound to fill the gaps between the surfaces and hence lower the contact thermal resistance. This compound also has the advantage that it prevents moisture from penetrating between the surfaces.

A number of different companies offer heatsinking compound, these usually consist of silicon grease loaded with some electrically insulating, good thermally conducting material such as alumina. Thinly applied, these compounds are advantageous as they fill the air gaps and do not further increase the distances between the surfaces. Thickly applied they can hold the two surfaces apart and increase the contact thermal resistance. The following graph displayed in Figure 1.4 shows the contact thermal resistance for 'dry' conditions (no compound) and the thermal resistance using compound, both are plotted against contact force.

The metal heatspreader on the back of the SUPER-247 package is non-electrically isolated from the pinouts of the device within, *i.e. in the case of a MOSFET the heatspreader is the drain contact, for an IGBT the collector*. Hence in cases where devices are not electrically paralleled but share the same heatsink, it is necessary to insert an electrically isolating material between the package and the heatsink block. The isolator usually takes the form of a pad and many companies offer a range of pad material types and sizes dependant on requirements.



At the minimum stated contact force of 20 N the following contact resistances can be achieved:

Contact Conditions	$R_{th(c-s)}$ @ 20N Contact Force
'Dry' (no compound)	1.2°C/W
Thermal Compound	0.2°C/W

The pad obviously has a direct and detrimental effect on the contact resistance as insertion adds an extra resistance into the build-up. Again, the contact thermal resistance is dependant on contact pressure. The following graph, shown in Figure 1.5, illustrates the higher thermal resistance when using an isolator pad, adding a new line to the thermal resistance curve. The isolator used to plot the line was a typical silicone loaded pad. Therefore, it should be noted that when electrically isolating a device from a heatsink the thermal resistance of the system will increase.

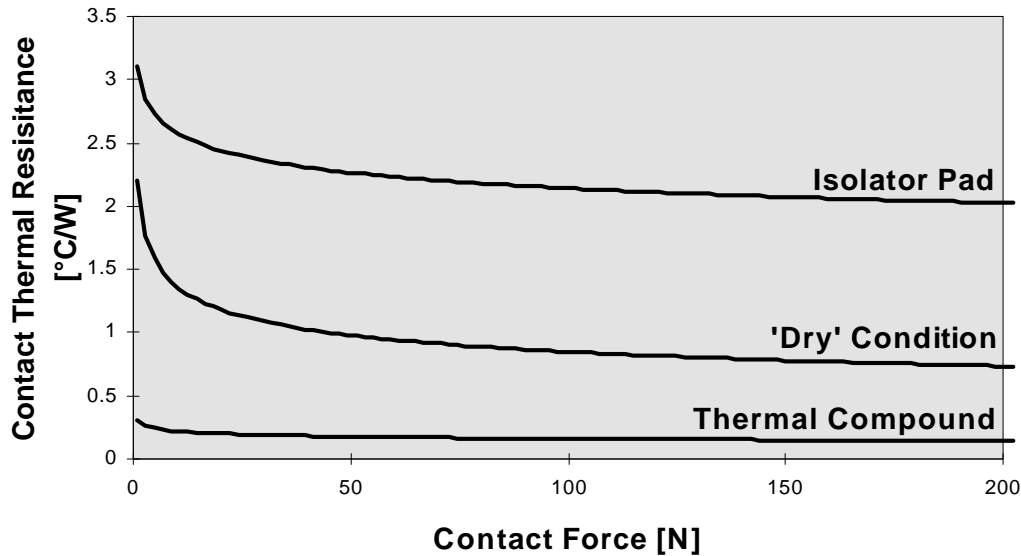


Figure 1.5 - Contact Thermal Resistance Plotted Against Contact Force

4. Typical Clips and What They Do

Why Clips?

The use of clips for providing the contact pressure is quickly becoming popular. Clip mounting provides a number of advantages over the more traditional screw mounting techniques:

- **Clips provide a more uniform pressure** over the entirety of the mating surfaces. Although screw mounting can provide a higher pressure, the force is centred at one end of the package and there is often a loss of coplanarity between package and heatsink.
- **Clips are faster to apply** than aligning and tightening screws.
- **Clips regulate the force applied** and ensure that the same force is applied to each package/heatsink pair. Hence there is no danger of over-tightening (deforming the package and/or heatsink) or under-tightening (increasing the contact thermal resistance).

Clip Types

There are a number of different clip types available on the market that can be used dependant on the application. Following are some examples of clips and the way in which they are typically used. The ideas shown by no mean encompass all the solutions available and do not prescribe the only ways in which the clips can be used.

Saddle Clips

An example of a SUPER-247 mounted to a heatsink using a saddle clip is shown in Figure 1.6.

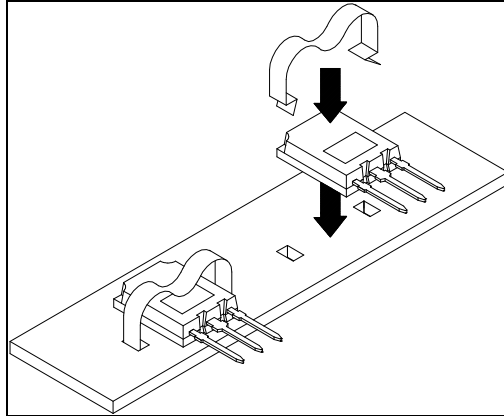


Figure 1.6 - SUPER-247 Mounted to Heatsink Using Saddle Clip

When using saddle clip type solutions, the heatsink materials are thin in cross-section, typically less than 5mm in thickness. The clips push into holes cut into heatsink material and lock against the back face of the heatsink. These clips produce contact forces in the range 20-60N.

'U' Clips

An example of a 'U' Clip assembly is shown in Figure 1.7.

This clip type clamps the device and the heatsink material together. Variations on this clip type allow devices to be clamped to the front and back of the heatsink block using the same clip. 'U' clips typically impart forces in the 20N-40N range. This force is partly dependent of the thickness of the heatsink material, *i.e. thicker the material, the greater the force.*

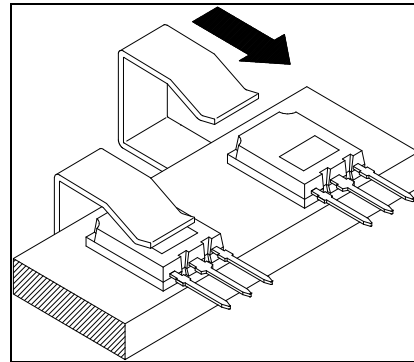


Figure 1.7 - 'U' Clip Assembly

Extrusion Mounted Clips

There are a number of proprietary clip solutions offered where the clip is anchored in a feature in the extruded heatsink. Figure 1.8 shows one solution type where the clip fits into a shaped slot in the heatsink material.

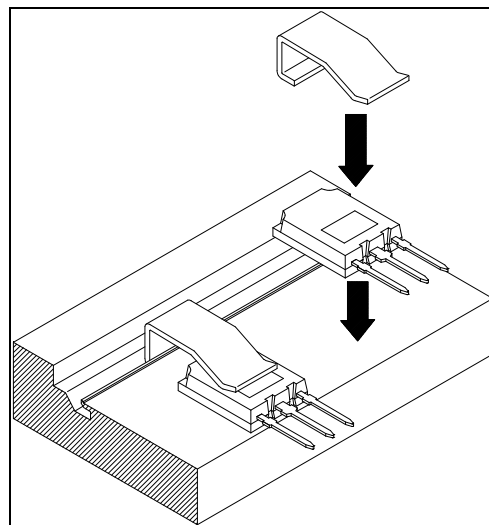


Figure 1.8 - Extrusion Mounted Clip (Slot Anchorage)

This solution can produce contact forces in the range 15 - 25N. However the shaped slot is an expensive addition to the heatsink and this solution type is being replaced in favour of clips mounted between shortened heatsink fins or clip rails (as shown in Figure 1.9 below). The extruded heatsinks are less costly and the forces that can be applied are higher, typically in the range 25 - 50N

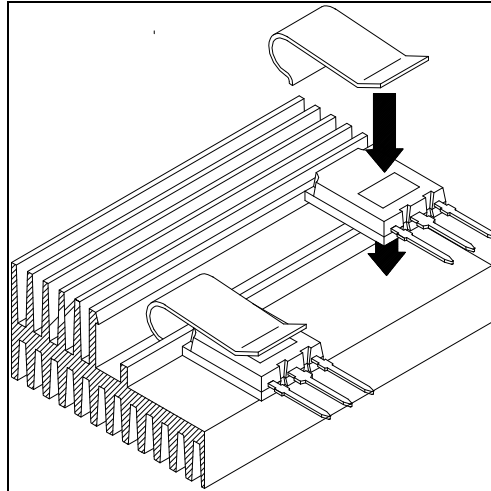


Figure 1.9 - Extrusion Mounted Clip (Rail Anchorage)

Other Solutions

Heatsink manufacturers offer a wide range of heatsink types, usually extrusions or formed metal and at a cost are willing to produce customised solutions. Some manufacturers will supply the heatsink with integrated clip both in extruded and formed metal varieties or a combination of the two. It is also possible to have heatsink solutions supplied with thermal compound or isolator materials already applied in the correct places to aid assembly.

Sources for Clip Solutions

The following are companies who can supply the types of clips/solutions discussed in this Application Note:

Redpoint Thermalloy,
Cheney Manor,
Swindon,
Wiltshire.
SN2 2QN

Aavid Thermal Technologies,
Corporate Headquarters,
One Kool Path,
Laconia,
New Hampshire
USA

Austerlitz Electronic gmbh,
Ludwig Feuerbach -Straße 38,
90961 Nüenburg, Postfach 1048,
GERMANY

Relevance to TO-247 Heatsink Mounting

The clipping/mounting concepts covered in this application note for the SUPER-247 can also be applied to the standard TO-247 package. However, it should be noted that due to the screw mounting capability of the standard TO-247 the package to heatsink contact area is reduced and hence the contact thermal resistance is **INCREASED** from $0.2^{\circ}\text{C}/\text{W}$ (SUPER-247) to $0.24^{\circ}\text{C}/\text{W}$ (TO-247). Therefore, whilst the minimum clamping force of 20N still applies, the contact thermal resistance graph for the SUPER-247 will not.

Conclusion

The SUPER-247 package can now dissipate more power and encapsulate more silicon than the industry standard TO-247, a package with the same footprint. It also allows for faster and less costly clip mounting to heatsinks. However, the way in which the device is mounted to the heatsink will affect the thermal performance of the system (silicon, package and heatsink). The designer can have a direct affect on the contact thermal resistance and the design parameters that he sets can have either a positive or adverse effect on system performance. This Application Note has discussed the need for an adequate force (20N) for good thermal contact and the fact that intermediate materials also affect the thermal resistance. Thinly applied thermal compound will improve the contact thermal resistance whilst electrical isolators are likely to cause deterioration in this parameter.

There are many clip/heatsink solutions available and some have been indicated in this Application Note. The chosen solution will depend on the application in which it is used and should be chosen to optimise both cost and thermal performance characteristics.

CALCULATING TEMPERATURE GRADIENTS IN POWER MOSFETS WITH THE “HEXRISE[®]” PROGRAM

by Doug Butchers, International Rectifier GB Ltd.

(HEXRISE[™] may be downloaded from: www.irgb.co.uk)

INTRODUCTION

This note is intended to assist with the application of the Program “HEXRISE[™]” in practical real life cases.

To use this Program effectively it is important to appreciate its scope and to be able to apply it to thermal calculations for heat sinking arrangements that extend beyond just the immediate boundaries of the power semiconductor itself.

Semiconductor cooling

A typical cooling arrangement for a power semiconductor device will involve the transfer of heat from its source (the junction) through many different materials and interfaces to the final cooling medium - usually air. Along the way, the generation of the temperature gradient of the junction above the ambient temperature, is a function of both the power flow and the thermal response to the different materials encountered in its course.

Figure 1 shows a typical mechanical arrangement for a plastic package on a heat sink. In many cases it would be usual to have an additional isolation layer between the base of the power semiconductor and the heat sink –especially for connections requiring multiple devices.

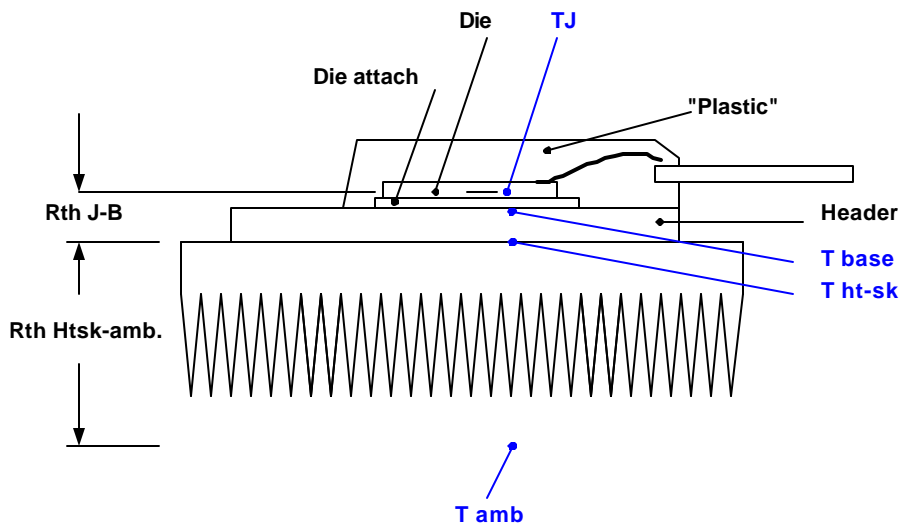


Figure 1: Typical heat sink arrangement

Equivalent thermal circuit

Figure 2 shows an equivalent thermal circuit for the previous mechanical example with the power semiconductor having two significant thermal components-the die and the package header.

There are two parameters associated with each different material section in the thermal path:

1. A thermal resistive element, R_{th} in K/W
2. A thermal capacity element, C_{th} in Ws/g.K

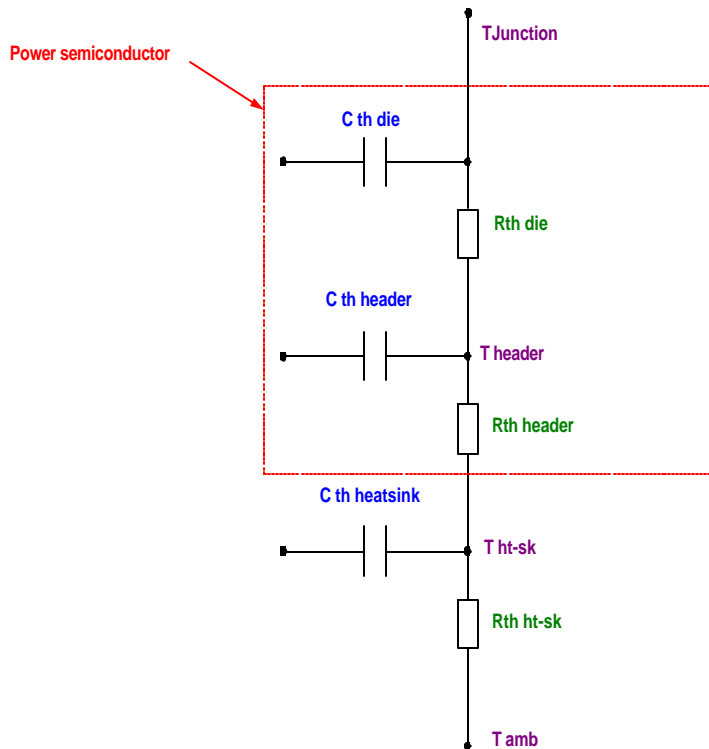


Figure 2: Equivalent thermal circuit

The thermal resistance element is responsible for the steady-state temperature difference across the section in question while the thermal capacity element is responsible for storing heat energy at a given rate, thereby introducing a time function which delays the establishing thermal gradient.

The combination of these two elements has a direct analogy to an electrical circuit containing resistance and capacitance. The $R_{th} \times C_{th}$ product is the thermal time constant with similar properties to the electrical time constant.

Alternative thermal approach

With HEXRISE™, the thermal response characteristics of the semiconductor is modelled in a more easily accessible way than above. The device thermal parameters (steady-state and transient) are derived from the data sheet transient resistance characteristic - readily available from every device data sheet. (more in the following section.)

Also, unlike the equivalent thermal circuit, the use of the data sheet thermal resistance characteristics makes a knowledge of the **separate** die and header thermal performance parameters unnecessary since the curve reflects the true transient and steady-state performance of the composite packaged part.

Basic Program principles

The temperature rise for a given thermal path in response to a power step such as that shown in figure 3, is given by:

$$\text{Temp rise @ } t_1 = P_1 \times R_{th1}$$

Where: P_1 the power
 R_{th1} is the thermal resistance @ time t_1

$$\text{The temperature rise @ } t_2 = P_1 \times R_{th2} - P_1 \times R_{th1}$$

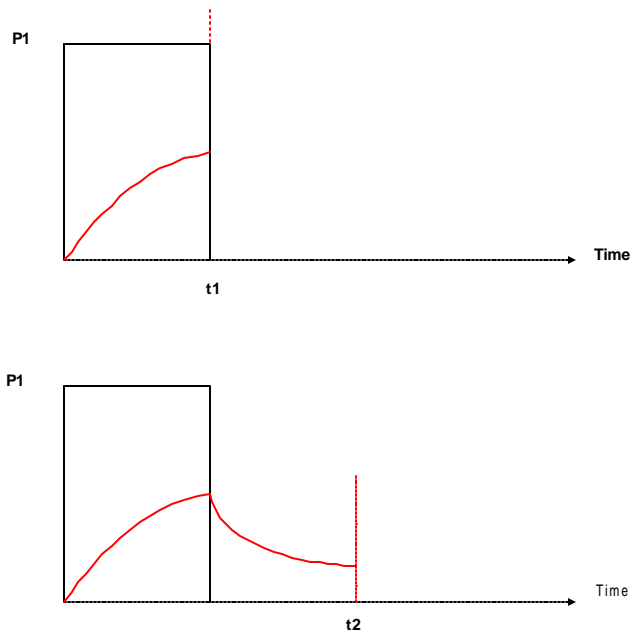


Figure 3: Basic temperature rise calculation

Any current waveform may be approximated by subdividing it up into small sections of time and specifying each subdivision with a power value and a thermal resistance value appropriate to the time at which it occurs. Refer to figure 4.

In this way, the temperature rise at any time may be calculated by applying this principle of positive and negative power pulse contributions to describe the complete wave shape.

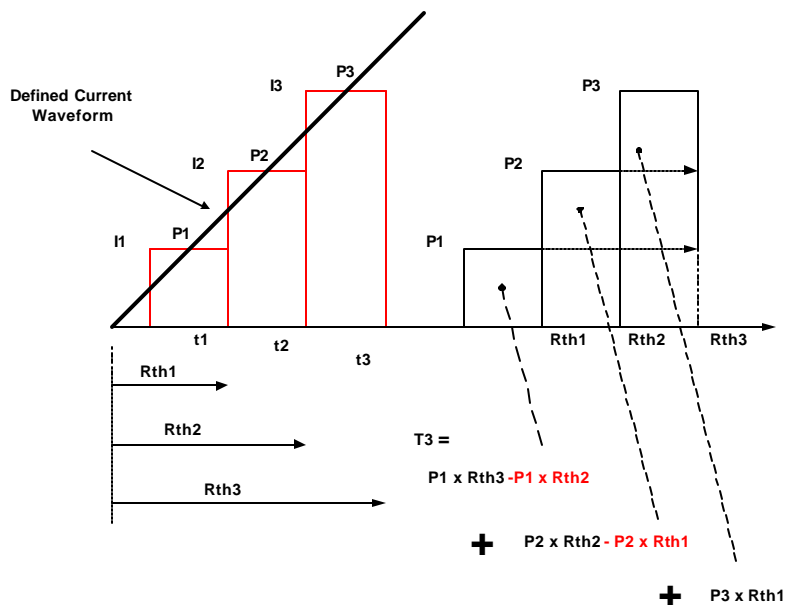
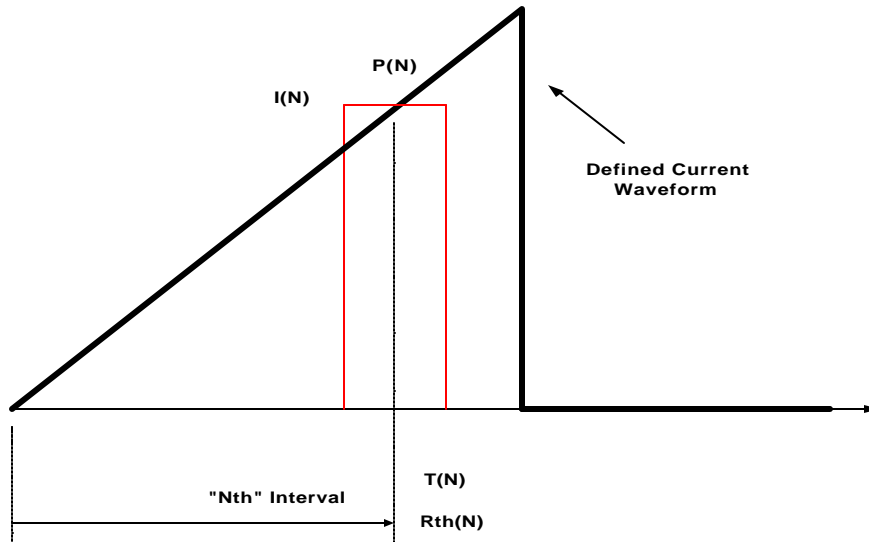


Figure 4: Waveform subdivision

General temperature rise expression

The temperature rise for the complete waveform can consequently be defined by a mathematical series such as that shown in figure 5. Note it is necessary to be able define the current waveform in terms of time for the purpose of calculating the instantaneous power.



$$T_N = P_1 (R_N - R_{N-1}) + P_2 (R_{N-1} - R_{N-2}) + P_3 (R_{N-2} - R_{N-3}) \dots + P_N R_1$$

- $T_{(N)}$ **is the temperature rise of the junction at the Nth interval**
- $P_{(N)}$ **is the instantaneous power in the device at the Nth interval using the mid-point current value**
- $R_{(N)}$ **is the transient thermal resistance (Junction-case) for the time $T_{(N)}$**

Figure 5: General series expression

Thermal resistance relationship

HEXRISE uses the transient thermal resistance characteristic from the device data sheet and relates it to time with the expression:

$$R(t) = XT \times T^{YT}$$

Where: $YT = \log (R1/R2) / (\log (T1/T2))$

$$XT = R / T^{YT}$$

Note that this calculation will only be valid for calculation times up to the “transient” characteristic limit indicated by the end of the “**straight line**” (Tlim) section of the published thermal resistance curve. Figure 6.

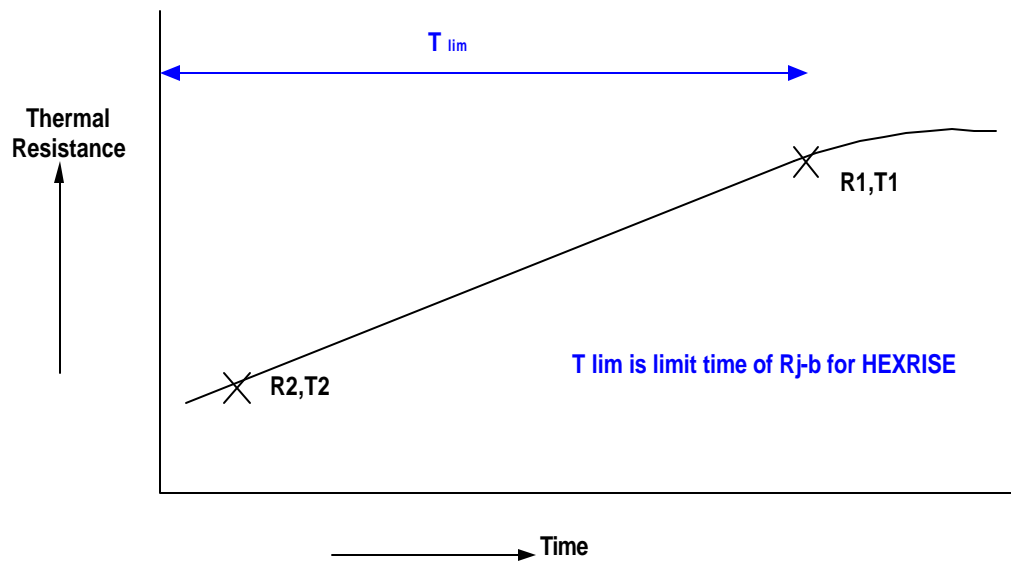


Figure 6: Data book thermal resistance curve (Log/Log scale)

Therefore for a defined current wave shape the temperature rise at a given time may be computed.

Program procedures

The Program computes as follows:

Calculates constants to express thermal resistance as a function of time (XT and YT)

Creates an array of thermal resistance values for each waveform subdivision (R_1 to R_N) and one of thermal resistance difference terms, $(R_N - R_{N-1})$ for the number of time intervals chosen.

Calculates instantaneous power values at each current / time subdivision of the waveform using the current expression as defined by the user. (P_1 to P_N)

Creates an array of Power x Thermal resistance difference terms for “N” time intervals $(P_1 \times (R_N - R_{N-1}))$ to $(P_N \times R_1)$

Sums all of the terms for temperature rise for each time interval. Refer to general expression in figure 5.

Using HEXRISE \bar{O} beyond the transient thermal resistance “limit”

The calculation is only accurate for calculation times up to the “transient” characteristic limit indicated by the end of the “straight line” (T_{lim}) section of the published thermal resistance curve. This can be the key area for accurate calculation as the junction-to-case thermal response is short compared with most heat sink response times and damage can occur to the silicon in these short times.

The HEXRISE™ program provides a means of accurately predicting the short-term temperature rise profile of the MOSFET (Junction-base) during this phase and can provide significant confidence in the long term reliability and integrity of the part in application.

In many applications the complete profile of the semiconductor’s absolute temperature depends upon the performance of the other heatsinking. Here it can be important to fully utilise both the steady-state and the transient thermal resistances of these coolers.

For example HEXRISE can also be usefully applied to longer-term high frequency application cases. Here the junction heating and cooling times are shorter in duration and the junction temperature *excursions* are smaller but the average power may well be relatively large. A significant temperature gradient may be developed across the cooling heatsink.

For continuous waveforms use the approach detailed in Application “profile 4” (next section) and run a 10-cycle calculation extrapolating it to a final settled value. This will provide an estimate for the maximum junction temperature excursion.

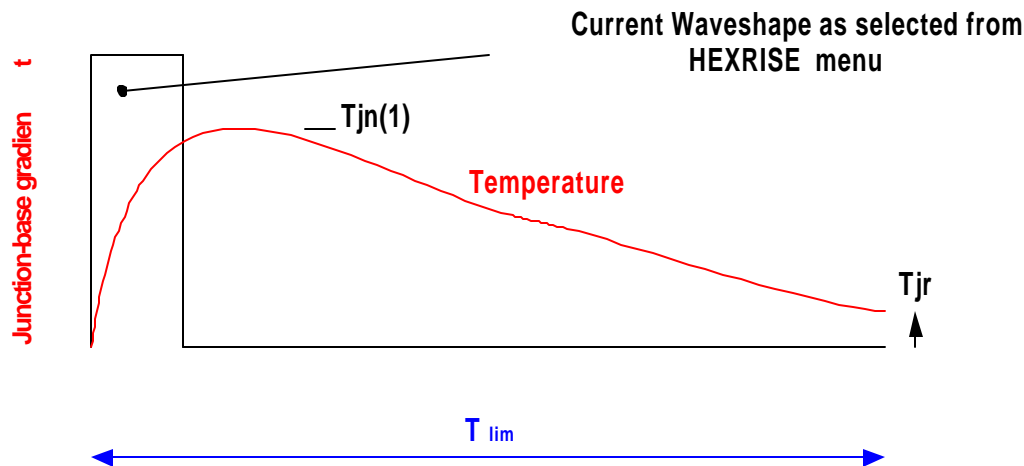
For a continuous high frequency waveform it will also be necessary to include switching losses and by adding these averaged power losses to the total losses and applying them to the heatsink gradient, the effect on the peak junction temperature may be included.

The section following shows how to combine the results from HEXRISE to those calculations where external heat sinking plays an important role.

Typical Application Profiles

Most applications where this Program will be helpful will have load duty cycles, which are characterised by one of the four following formats:

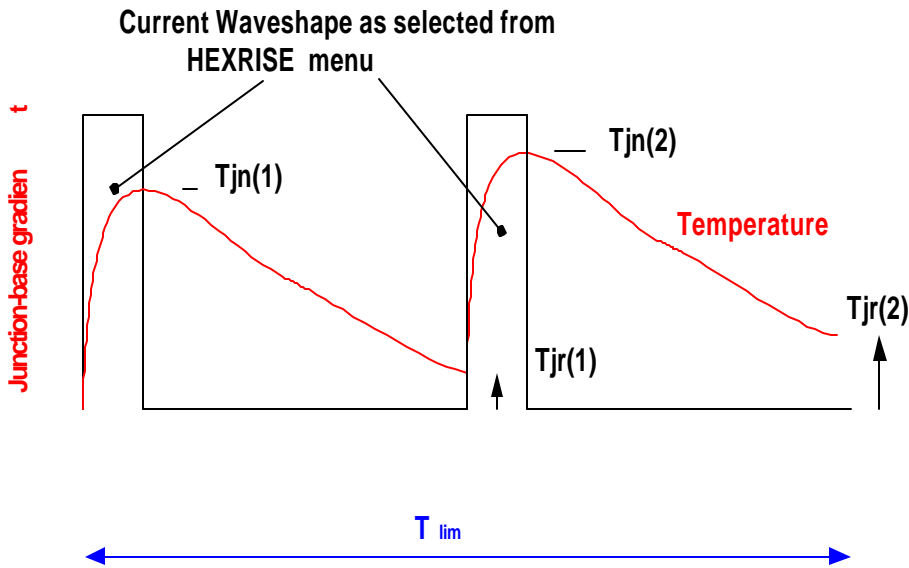
- 1. Single pulse of power within semiconductor transient R_{th} range (T_{lim})**



Key features

- On-time + off-time must be $\leq T_{lim}$
- Heatsink (if any) thermal performance is not significant here.
- Maximum absolute junction temperature will be $T_{jn}(1) +$ starting base / ambient temperature

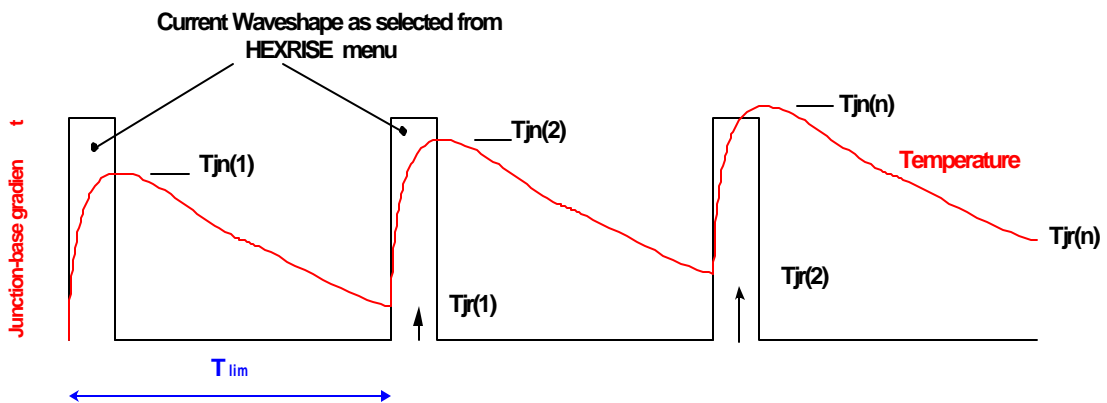
2. Multiple pulses of power within semiconductor transient R_{th} range (T_{lim})



Key features

- Total pulse train time must be T_{lim}
- Each successive peak temperature $T_{jn}(n)$ and residual cycle temperature $T_{jr}(n)$ is higher than the one before.
- Heatsink (if any) thermal performance is not significant here.
- Maximum absolute junction temperature will be $T_{jn}(n) + \text{starting base / ambient temperature}$

3. Multiple pulses of power for time greater than semiconductor transient R_{th} range (T_{lim})



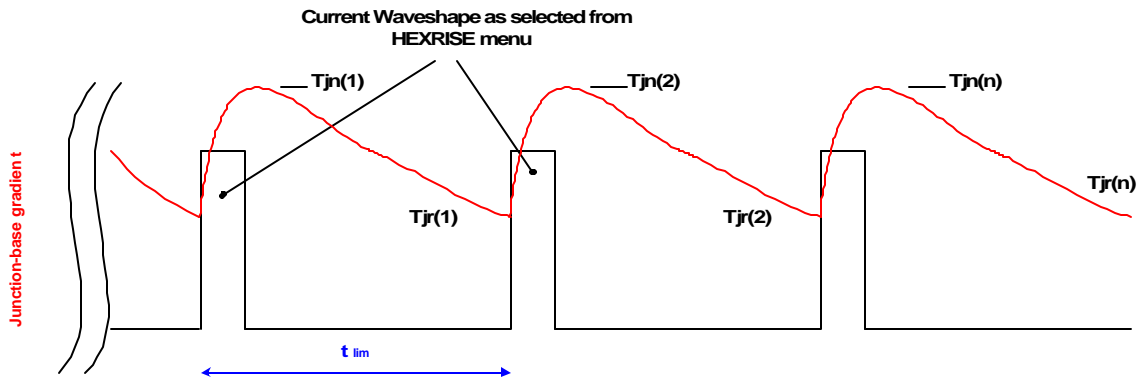
Key features

- Total pulse train time will be $\geq T_{lim}$
- Each successive peak temperature $T_{jn}(n)$ and residual cycle temperature $T_{jr}(n)$ is higher than the one before. A stable (equal) cycle temperature increase and cycle temperature decrease is not achieved.
- Heatsink thermal performance (transient thermal resistance) may be significant here.
- The maximum absolute junction temperature may be estimated for the nth pulse as:-
 $\cong (T_{jn}(n) - T_{jr}(n)) + W \times R_{thsk}(t) + \text{ambient temperature}$

W is the average power dissipated in the heatsink over transient time.

$R_{thsk}(t)$ is the heatsink **transient** thermal resistance for time (t) to the nth pulse.

4. **Multiple pulses of power for time which achieves steady-state thermal resistance for the heat sink and stable semiconductor temperature cycle increases and decreases.**



Key features

- Stable condition exists where $T_{jn}(1) = T_{jn}(n)$
- The maximum absolute junction temperature may be estimated as:

$$(T_{jn}(n) - T_{jr}(n))^{**} + W \times R_{thsk}(s/s) + \text{ambient temperature}$$

$R_{thsk}(s/s)$ is the heat sink steady-state thermal resistance.

W is the average power dissipated in the heat sink

** Run HEXRISE for sufficient time to be able to identify stability

In all cases considered, the thermal time constant of the heat sink is assumed to be long compared with that of the semiconductor device.

Summary

The junction temperature profile of a power MOSFET for a variety of applied current waveforms may be predicted using the HEXRISE[®] Program.

Short-term temperature effects are calculated directly, while for the longer and continuous events, transient and steady-state temperature rises (determined by relatively large external heatsinks) may be combined with these short-term profiles to arrive at an accurate assessment of the instantaneous junction temperature.

The approach taken in HEXRISE[™] very specifically uses data sheet information and thereby deliberately avoids the need for the inclusion of constructional-related details of die and package - not always readily available to the user.

The benefits of being able to assess peak temperature excursions for a variety of applied current waveforms are that reliability and even survivability judgements may be made with some degree of accuracy.

In many applications, such are the economic pressures upon designs, that occasional, severe short-time overloads may have to be accommodated with components whose size or number cannot be increased. A confidence in the maximum temperature peaks and their duration is essential in accurate risk assessment.

HEXRISE[™] provides a screen driven format, which enables the user to view the chosen defined current waveform and immediately appreciate the resulting graphical temperature profile.

MOSFET Thermal Characterization in the Application

Wharton McDaniel

INTRODUCTION

The use of surface-mount packages for power MOSFETs has progressed dramatically over the past 10 years. Today, power MOSFETs are widely available in packages that continue to get smaller. Now the question is how to choose best device in the smallest package and make a space-critical design as effective as possible. A major part of the problem is determining the thermal performance of the device on the printed circuit board (PCB) where it is mounted. Fortunately, a simple test method can be used to establish thermal performance of a MOSFET in a particular application.

THERMAL CHARACTERIZATION DATA

The main piece of thermal data provided by MOSFET suppliers is typically $R_{\theta JA}$, or junction-to-ambient thermal resistance. The basic thermal circuit (Figure 1) for this parameter consists of two components: the thermal resistance of the package and the thermal resistance of the PCB it is mounted on. The problem with the PCB component in $R_{\theta JA}$ is that the characterization board used to create data sheet specifications does not accurately represent the boards used in actual applications. The PCB area is different, the copper patterns are different, many applications use multilayer board, and actual applications have many different components mounted on the board along with the MOSFET. All these things create thermal performance that tends to be different, and in most cases better than the performance of the characterization board. More recently, suppliers have added $R_{\theta JF}$ to the characterization data, which defines the thermal performance of the package itself. This is an excellent parameter to use to compare package performance and to use in determining actual device performance.

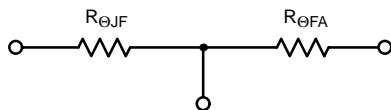


FIGURE 1. Basic Thermal Circuit

THERMAL PERFORMANCE IN THE APPLICATION

For any given application, the ideal MOSFET is the smallest device that provides the electrical and thermal performance that is required. The thermal performance is the most difficult to predict since, as previously described, the thermal characteristics of each PCB are different. Although there is data published showing the relationship between thermal resistance and the copper area used to spread heat, it is

accurate only for the PCB where it is mounted. When trying to optimize the thermal performance, this is not good enough.

The most practical method of optimizing thermal performance is to characterize the MOSFET on the PCB where it will be used, or on a board that is very similar. This characterization can be performed using the same techniques used for the datasheet characterization, although the datasheet characterization is performed by a dedicated thermal analyzer. The basis of this method is to dissipate a known amount of power in the MOSFET, and to measure the amount of temperature rise this causes in the junction, giving the data required to calculate the junction to ambient thermal resistance in $^{\circ}\text{C}/\text{W}$. The following procedure provides a simple method of determining the steady-state thermal resistance of a MOSFET on the PC board where it will be used.

THERMAL CHARACTERIZATION PROCEDURE

The procedure has two main steps. First is the characterization of the body diode. Second is the temperature rise measurements and calculation of the thermal resistance.

Diode Characterization

Characterization of the body diode is important because the body diode is used to measure the junction temperature of the MOSFET. As an inherent part of the MOSFET structure, the body diode makes the ideal sensor for this purpose. The forward voltage, V_F , of the diode varies with temperature, therefore the diode's temperature coefficient is needed to get an accurate representation of the junction temperature. The forward voltage is measured with a low level current flowing through it to insure there is no self heating, which would make the junction temperature measurement inaccurate. If it is not possible to perform the measurements of V_F , the generic V_F temperature coefficient of $-2\text{mV}/^{\circ}\text{C}$ for a diode can be used at the cost of accuracy.

For characterization of the diode, the MOSFET can be mounted on a PCB or just connected with wires. Electrically, the gate should be connected to the source to insure the MOSFET cannot turn on.

The characterization is performed as follows:

- Measure room temperature T_{room}
- Measure V_F of body diode with I_F of 10 mA at room temperature
- Measure V_F of body diode with I_F of 10 mA at 100°C
- Calculate the diode temperature coefficient using

$$T_C = \frac{V_F @ 100^{\circ}\text{C} - V_F @ \text{room}}{100 - T_{\text{room}}} \text{ (mV}/^{\circ}\text{C)}$$

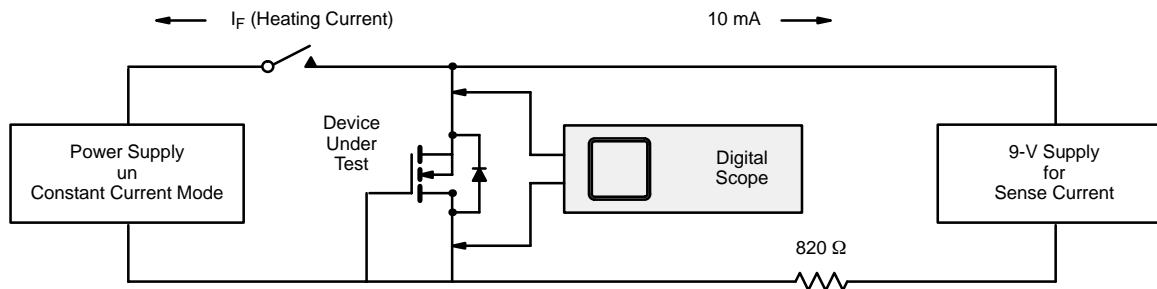


FIGURE 2. Connection Diagram

Temperature Rise Measurement and Calculation of Thermal Resistance

The MOSFET being characterized is mounted on the application PCB and has the gate shorted to the source, with the drain and source connected to two power supplies (Figure 2). The first power supply is configured as a constant current source, which forces current through the body diode to heat the junction when the switch is closed. The second power supply provides the sensing current for measuring the junction temperature. This supply is connected to the drain and source, forcing 10 mA through the body diode, with the V_F of the body diode indicating the junction temperature. Also, it stays connected throughout the test in order that the sensing current will flow immediately upon removal of the heating current.

The measurement procedure is as follows:

- Close the switch.
- Source current through the body diode such that approximately 1 W is dissipated after reaching equilibrium. Equilibrium has been reached when V_F stabilizes.
- Power is defined as $P_D = V_F \times I_F$.
- Open the switch, dropping I_F to 10 mA. Measure V_F immediately using a digital scope triggered on the negative slope of V_F .

Calculation of $R_{\theta JA}$

- Calculate ΔV_F , result will be negative
- Calculate ΔT_J using $\Delta T_J = \Delta V_F / T_C$
- $R_{\theta JA} = \Delta T_J / P_D$

Verification of the Method

This method was verified using an Si4410DY mounted on the standard thermal characterization board. The forward voltage of the body diode, V_F , was measured to be 0.586 V at a room temperature of 21.3°C. The device was placed in an oven, the oven temperature raised to 100°C, and V_F measured to be 0.394 V. This yields

$$T_C = \frac{0.394 \text{ V} - 0.586 \text{ V}}{100^\circ\text{C} - 21.3^\circ\text{C}} = -2.4 \frac{\text{mV}}{^\circ\text{C}}$$

With the device connected according to Figure 2, 0.94 W was dissipated in the body diode. The starting value was measured to be 0.582 V. A digital oscilloscope was used to measure V_F immediately after the heating current was turned off. This gave a V_F of 0.402 mV. ΔV_F is -180 mV . Therefore,

$$\Delta T_J = \frac{\Delta V_F}{T_C} = \frac{-180 \text{ mV}}{-2.4 \frac{\text{mV}}{^\circ\text{C}}}$$

$$\Delta T_J = 75^\circ\text{C}$$

and

$$R_{\theta JA} = \frac{\Delta T_J}{P_D} = \frac{75^\circ\text{C}}{0.94 \text{ W}}$$

$$R_{\theta JA} = 79.8 \frac{^\circ\text{C}}{\text{W}}$$

This value compares well with the measured value of 75.7°C/W , measured using an AnaTech Phase 10 analyzer.

With $R_{\theta JA}$ calculated, junction temperature can be predicted for any given power dissipation level using the equation as previously mentioned.

$$T_J = P_D \times R_{\theta JA} + T_A$$

It should be noted that if other components on the PCB generate heat, the effective $R_{\theta JA}$ will be higher since the temperature of the PCB will be raised by those components. If those components can be made to dissipate their typical power while performing the characterization above, the value of $R_{\theta JA}$ will reflect this additional heating.

CONCLUSION

The process of selecting a power MOSFET on the basis of electrical parameters must be done with care. Close attention must be paid to the thermal performance of the MOSFET as part of the PCB assembly. Characterization of the MOSFET being used on the PCB being used can help insure that the correct device is chosen on the basis of both electrical and thermal performance.